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Calibration of models for III-V TFET performance prediction

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Prof. Carlo Vandecasteele, chair
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Dissertation presented in partial fulfillment of the requirements for the degree of Doctor in Engineering Science (PhD): Materials Engineering

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Abstract

Since the fabrication of the first Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) in 1960, we have witnessed a tremendous increase in computational performance, driving worldwide technological innovation. This increase in performance was and is still possible by systematically downscaling the dimensions of the MOSFET, the basic building block of integrated circuits. Today, maintaining this scaling trend has become increasingly difficult, because the power consumption of the MOSFET can no longer be lowered sufficiently.

Therefore, we investigate whether the Tunneling Field-Effect Transistor (TFET) is a viable alternative to the MOSFET for low-power integrated circuits. The carrier injection mechanism of the TFET is quantum mechanical Band-To-Band Tunneling (BTBT). This is accompanied by an energy filtering mechanism, which allows switching from the off-state to the on-state using a lower supply voltage than MOSFET, and hence reducing the power consumption of integrated circuits.

To identify favorable III-V TFET configurations and guide TFET fabrication, semi-classical and quantum mechanical simulations are crucial. However, there is uncertainty on the accuracy of the relevant models and the input parameters. Therefore, the topic of this thesis is the experimental calibration of these models. We achieve this using tunnel diodes and MOS capacitors, which are simpler to fabricate and characterize than complete TFETs.

This allows us to decouple the different effects occurring in a TFET. We identify the desired current components due to BTBT, but also parasitics like Shockley-Read-Hall generation and trap-assisted tunneling due to bulk traps. We also identify dopant- and temperature dependent bandgap narrowing, the energy band alignment of heterojunction TFET and field-induced quantum confinement. We then calibrate the relevant models in semi-classical and quantum mechanical simulators. Our work enables improved understanding of experimental TFET data and more accurate performance prediction of III-V heterojunction TFET.

Beknopte samenvatting

Sinds de fabricatie van de eerste metaal-oxide-halfgeleider veldeffecttransistor (MOSFET) in 1960, hebben we dankzij technologische innovatie jaar na jaar kunnen rekenen op een exponentiele toename van de rekenkracht van computers. Vandaag de dag wordt het steeds moeilijker om deze trend verder te zetten, omdat het vermogenverbruik van de MOSFET niet verder verlaagd kan worden.

Daarom onderzoeken we of de tunneling-veldeffecttransistor (TFET) de MOSFET kan vervangen, om zo een lager vermogenverbruik te bereiken. Het ladingsinjectiemechanisme van de TFET is band-tot-bandtunneling (BTBT), wat gepaard gaat met een energiefilteringmechanisme. Dankzij deze filtering is het mogelijk om te schakelen van de uit- naar de aan-toestand bij een lagere bronspanning. Dit verlaagt het vermogen verbruik van geïntegreerde circuits.

Om de meest beloftevolle TFET configuraties te identificeren en om experimenteel onderzoek te ondersteunen zijn semiklassieke en kwantum mechanische simulaties cruciaal. Er is echter onzekerheid over de nauwkeurigheid van de relevante modellen en op de bijhorende inputparameters. Het onderwerp van dit onderzoek is de experimentele kalibratie van de modellen voor de gewenste BTBT stroom, maar ook parasitaire mechanismen zoals Shockley-Read-Hall (SRH) en defect-geassisteerd tunnelen (TAT). We karakteriseren ook veld-geïnduceerde kwantum opsluiting (FIQC) en de alignatie van de energiebanden in heterostructuur TFET. Dit gebeurt met MOS capaciteiten en tunneldiodes. Deze halfgeleidercomponenten zijn gemakkelijker te fabriceren en te karakteriseren dan volledige TFETs. Dankzij ons onderzoek is het mogelijk om de prestatie van III-V heterojunctie TFET nauwkeuriger te voorspellen en experimentele resultaten beter te begrijpen.

Preface

I would like to express my sincerest gratitude towards my daily supervisor Dr. Anne Verhulst. Since day one she taught me to focus only on the most relevant topic, and set up a strategy before starting a new experiments or a simulation. She helped me to consistently improve the quality of my research. She always gave me her honest opinion about my presentations and my way of working, and she reviewed all my publications and this PhD manuscript in great detail. I want to thank her for her guidance and her great personal commitment. I couldn't have wished for a better daily supervisor.

I am grateful to my supervisor Prof. Marc Heyns for introducing me to the TFET subject, inspiring me about the amazing field of nanotechnology, and helping me to think out of the box. I thank Rita Rooyackers for her valuable experimental guidance. I am grateful to IWT and all the Flemish taxpayers for funding my PhD, and to imec and the TFET project managers Dr. Nadine Collaert, Dr. Anda Mocuta and Dr. Aaron Thean for making this research possible. Thank you Salim, Clement, Cedric, Geoffrey, Frank, Anne Vandooren, Devin, Caio, Alireza, Amey, Abhitosh, Tsvetan, Mazhar, Ashish and Jasper for the great collaboration and the pleasant work environment. I thank Kim, Johan and Johan for the excellent technical support in the III-V clean room. Thank you Rita and Alireza for proofreading chapters of my PhD manuscript. Thank you Eddy, Devin, Maarten, Salim, Koen, Dennis for the many scientific discussions and for proofreading publications.

Dr. David Gundlach, thank you for offering me the guest researcher position at NIST, for teaching me not to fear cryogenics, and for passing over some of your true creative experimentalist spirit. You were a great supervisor. Thank you Dr. Charles Cheung for the in-depth discussions on pulsed I-V. Thank you Rahul Pandey and Prof. Suman Datta for the excellent TFET samples and the collaboration. I am grateful to Nhan and Oleg from NIST for introducing me to IPE measurements, and to Ji-Hong, Jason, David, Dmitry and Pragya helping me setting up the pulsed I-V experiments, soldering circuits and achieve impedance matching.

I am grateful to my US friends Leandro, Alice, Bela, Robert, Kjell, Kevin, James, Joe, Son, Adam for the many Barbecue Fridays, the Indonesian gastronomy, the many interesting discussions about US vs Europe, the horror movie nights and other great times in DC. I want to thank Maarten, Maarten and Devin for being great friends and colleagues. Thank you Diederick, Tom, Pepe and Joel for the many years of friendship. I thank my parents for their guidance, for always being supportive, and for all the opportunities they gave me. Thank you Dorien, my love, for sharing life with me.

In the spirit of our discussions at the lunch table, I present the following cartoon as an introduction to this thesis:

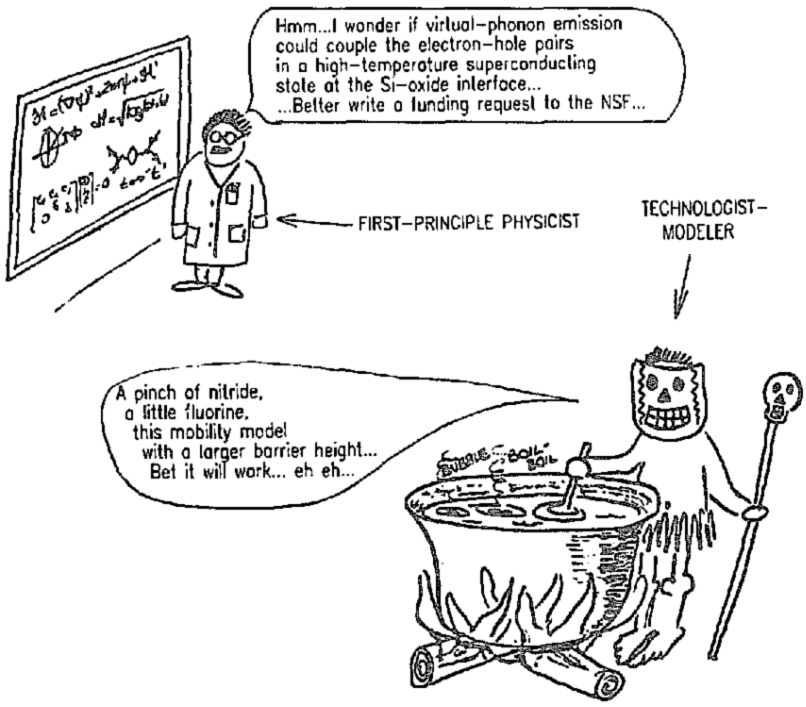

Figure 1: This thesis is about bridging the gap between TFET research by the first-principle physicist and the technology-modeler. Cartoon modified from M.V. Fischetti, S.E. Laux, D.J. Dimaria, "The physics of hot-electron degradation of Si MOSFET's: Can we understand it?" *Applied Surface Science*, **39**, 578 (1989)

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Abbreviations

All abbreviations are written in upright capitals. All symbols are variables or parameters, and start with a slanted letter or a Greek symbol.

AC	Alternating Current
ALD	Atomic Layer Deposition
BCB	Benzocyclobutene, dielectric interlayer
BHF	Buffered Hydrogen Fluoride
BTBT	Band-To-Band Tunneling
CVD	Chemical Vapor Deposition
DC	Direct Current
DOPBGN	Doping-dependent Bandgap Narrowing
DOS	Density Of States
EOT	Equivalent Oxide Thickness
FD	Fermi-Dirac
IPA	Isopropyl Alcohol
IX845	a positive tone photosensitive resist for i-line lithography
LOR1A	a resist that facilitates lift-off
MB	Maxwell-Boltzmann
MBE	Molecular Beam Epitaxy
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MPIV	Multi Pulse I-V
MS2001	a solvent used for resist strip and metal lift-off
NDR	Negative Differential Resistance
PBTI	Positive Bias Temperature Instability
PIV	Pulsed current voltage measurement
PVCR	Peak-to-Valley Current Ratio
PVD	Physical Vapor deposition
RIE	Reactive Ion Etching
SEM	Scanning Electron Microscopy
SPIV	Single Pulse I-V

SRH	Shockley-Read-Hall generation/recombination
TAT	Trap-Assisted Tunneling
TBGN	Temperature-dependent Bandgap Narrowing
TFET	Tunneling Field-Effect Transistor
TP	Transmission Probability
WKB	Wentzel-Kramer-Brillouin
XSEM	cross-section Scanning Electron Microscopy

List of symbols

All symbols are variables or parameters, and start with a slanted letter or a Greek symbol. All abbreviations are written in upright capitals.

Δt	time delay between *is* and *vg*: section 6.9.6 on p. 146
$\Delta\Psi_\mathrm{s}$	electrostatic potential drop over the semiconductor
$\Delta\Psi_\mathrm{s}^*$	$\Delta\Psi_\mathrm{s}$ at the onset of inversion: section 5.8 on p. 125
κ	imaginary part of wavevector: section 2.8 on p. 35
ξ_n	degeneracy of electron quasi Fermi level: section 2.2 on p. 26
ξ_p	degeneracy of hole quasi Fermi level: section 2.2 on p. 26
τ_AC	time constant of AC signal, $1/(2\pi f_\mathrm{AC})$: section 5.1 on p. 113
τ_BTBT	time constant of inversion charge by BTBT: section 5.4 on p. 117
τ_DC	time constant of DC signal change: section 5.1 on p. 113
τ_th	time constant for thermal generation of inversion charge
A_BTBT	BTBT parameter in Kane formalism: section 2.2.1 on p. 25
A_j	junction area: section C.8 on p. 195, section 3.3.4 on p. 61
B_BTBT	BTBT parameter in Kane formalism: section 2.2.1 on p. 25
C-V	Capacitance - Voltage
C_gd	gate to drain equivalent capacitance: figure 6.2 on p. 136
C_gs	gate to source equivalent capacitance: figure 6.2 on p. 136
C_gd^*	equivalent capacitance in floating source C-V: figure 6.2 on p. 136
C_gs^*	equivalent capacitance in floating drain C-V: figure 6.2 on p. 136
C_inv	inversion capacitance: section 5.8 on p. 125
C_ox	oxide capacitance
C_s	semiconductor capacitance: section 5.8 on p. 125
$C_\mathrm{s,min}$	minimum semiconductor capacitance: section 5.8 on p. 125
D_var	variation of the diode diameter by overetching: section 3.3.4 on p. 61
E_1	first subband energy level: section 5.1 on p. 113
E_g	bandgap
$E_\mathrm{g,eff}$	effective bandgap for heterojunction tunneling: section 1.5 on p. 13
E_c	minimum energy of the conduction band

E_{fn}	electron quasi Fermi level
E_{fp}	hole quasi Fermi level
E_{v}	maximum energy of the valence band
F	electric field
f_{AC}	AC frequency in C-V measurement
g	degeneracy factor
G	amplifier Gain: section 6.8
G_{BTBT}	BTBT generation rate: section 2.2.1 on p. 25
h	Planck constant, h=4.14 × 10^{-15} eV s
$\hbar$	reduced Planck constant, $\hbar$=6.58 × 10^{-16} eV s
is	source current waveform (in volts) at oscilloscope: figure 6.4(c) on p. 139
I	current
I_{disp}	displacement current: section 6.9.5 on p. 146
I_{ds}	transistor drain to source current
I_{p}	Esaki diode peak current: section 2.1.2 on p. 24
I_{s}	transistor source current
I_{v}	Esaki diode valley current: section 2.1.2 on p. 24
J	current density
J_{p}	Esaki diode peak current density
k_{B}	Boltzmann constant, k_{B}=8.62 × 10^{-5} eV K^{-1}
k	wavevector: section 2.8 on p. 35
L_{t}	tunnel path length
m_{e}	electron effective mass
m_{lh}	light hole effective mass
m_{hh}	heavy hole effective mass
m_{r}	Reduced tunnel mass
N_{A}	acceptor dopant concentration
N_{D}	donor dopant concentration
P	Power
p	pressure
q	elementary charge, q=1.60 × 10^{-19} C
R_{BTBT}	equivalent resistance of BTBT
R_{eq}	equivalent series resistance: figure 6.2 on p. 136
R_{d}	drain resistance in simplified C-V circuit: figure 6.2 on p. 136
R_{s}	source resistance in simplified C-V circuit: figure 6.2 on p. 136
R_{t}	tunnel junction resistance in simplified C-V circuit: figure 6.2 on p. 136
R_{q}	root mean square roughness
R_{p}	maximum peak height roughness
SR	Slew Rate: section 6.8 on p. 141
SS	Subthreshold Swing
SS_{min}	minimum-point Subthreshold Swing: section 1.3 on p. 10
t	time

t_{avg}	averaging time to reduce noise in PIV: section 6.9.1 on p. 143
t_{f}	time of falling edge: figure 6.4(a) on p. 139
t_{meas}	extraction time of *vgmeas*, *idmeas*: figure 6.4(e) on p. 139
t_{r}	time of rising edge: figure 6.4(a) on p. 139
T	temperature
T_{i}	thickness of the intrinsic region of p+/i/n+ diode: section 3.4.1 on p. 64
V	Voltage
V_{c}	corner point voltage in heterojunction diode: section 4.3.1 on p. 99
V_{d}	transistor drain voltage (not referenced)
V_{d0}	transistor drain to circuit ground voltage: section 6.7 on p. 138
V_{ds}	transistor drain to source voltage
vg	gate voltage waveform at oscilloscope: figure 6.4(c) on p. 139
vgmeas	value of *vg* at t_{meas}: figure 6.4(e) on p. 139
V_{g}	transistor gate voltage (not referenced)
V_{g0}	transistor gate to circuit ground voltage: section 6.7 on p. 138
V_{gs}	transistor gate to source voltage
V_{np}	diode reverse bias voltage
V_{p}	peak voltage: section 2.1.2 on p.24
V_{s}	transistor source voltage (not referenced)
V_{v}	valley voltage: section 2.1.2 on p. 24
W_{i}	width of diode with index i: figure C.2 on p. 178

Chapter 1

Introduction

1.1 MOSFET scaling and operation principle

Since the fabrication of the first Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) in 1960 [1], we have witnessed a tremendous increase in computational performance, driving worldwide technological innovation. This increase in performance was and is still possible by systematically downscaling the dimensions of the MOSFET, the basic building block of integrated circuits. As a result, the number of MOSFETs in integrated circuits doubles every two years. This observation was initially made by Gordon Moore in 1965 [2], revised in 1975, and since then known as *Moore's law*. In 1971, Intel's *4004* cpu consisted of 2300 interconnected MOSFETs with a minimum feature size of 10 µm. Today's high-end cpu's consist of billions of interconnected fin-shaped MOSFETs with 8 nm fin width and 42 nm fin pitch [3].

However, this tremendous increase in MOSFET density was not without issues, and an enormous research investment is made for every new generation of integrated circuits. Today, the main roadblock limiting downscaling of the MOSFET is the increasing power density. This PhD thesis is a part of the research effort to decrease the power consumption of the basic building block in integrated circuits.

The main cause of the increasing power density in the MOSFET is the subthreshold leakage current. In the MOSFET transfer characteristics, sketched in figure 1.1(d), the drain-source current I_{ds} in the subthreshold region increases exponentially with the gate-source voltage V_{gs}, with a fixed subthreshold swing $SS{=}\mathrm{d}V_{\mathrm{gs}}/\mathrm{d}\,\log_{10}(I_{\mathrm{ds}}){\geq}60\,\mathrm{mV/dec}$. The cause of the subthreshold current

can be understood from the energy band diagram in figure 1.1(c), where the Fermi-Dirac electron occupation is schematically depicted in shades of red. Most source electrons are blocked by the potential barrier in the channel, but the high energy electrons in the Fermi-Dirac tail are injected into the channel by thermionic emission. This causes $SS \geq \ln(10) k_B T/q = 60\,\text{mV/dec}$ at room temperature, where T is the temperature, k_B is the Boltzmann constant and q is the electron charge.

When a new MOSFET technology node is developed, and the dimensions are scaled down by a certain factor, V_{dd} must be decreased by the same factor to keep the power density constant. But in today's MOSFETs, further lowering V_{dd} is accompanied by either an increased I_{off} or a decreased I_{on} due to the fixed $SS \geq 60\,\text{mV/dec}$. If a circuit engineer decides to operate the MOSFET at higher I_{off}, the leakage current and therefore the power density increases. If, on the other hand, the circuit is operated at lower I_{on}, this induces a longer delay to charge the next transistor in the circuit and hence less operations can be performed in the same time. This trade-off between both components is captured by the energy-delay product for logic operations [4]. The increasing power density for smaller MOSFETs is a therefore a fundamental issue. Hence we investigate the feasibility of the Tunneling Field-Effect Transistor (TFET), a radically new type of transistor.

1.2 TFET operation principle

The desired transfer characteristics in figure 1.1(d) show an optimized TFET achieving a similar I_{off} and I_{on} as LP MOSFETs, while operating at lower V_{dd}. I_{off} and I_{on} will be defined in section 1.3. Circuit simulations of a 32-bit adder by Nikonov *et al.* [4] have shown that homojunction and heterojunction TFETs offer about 100× lower energy-delay product than low-power (LP) CMOS, mainly because the TFET is not limited to a swing $\geq 60\,\text{mV/dec}$.

The steep switching, related to the TFET's carrier injection mechanism which is BTBT, is explained in the coming paragraphs. Figure 1.1(e) shows the most common n-TFET configuration, which is a reverse biased p+/i/n diode with a gate stack over the intrinsic region. Deep in the bulk of the TFET (figure 1.1(h)), the gate has no control over the electrostatic potential. The tunneling paths are long, and BTBT is negligible when the intrinsic region is longer than 50 nm for $In_{0.53}Ga_{0.47}As$ TFET. This value is obtained from BTBT current density measurements in figure 3.9 on p. 72.

In the TFET on-state (figure 1.1(f)), the gate voltage is high and the conduction and valence energy bands in the channel near the gate move to lower energy.

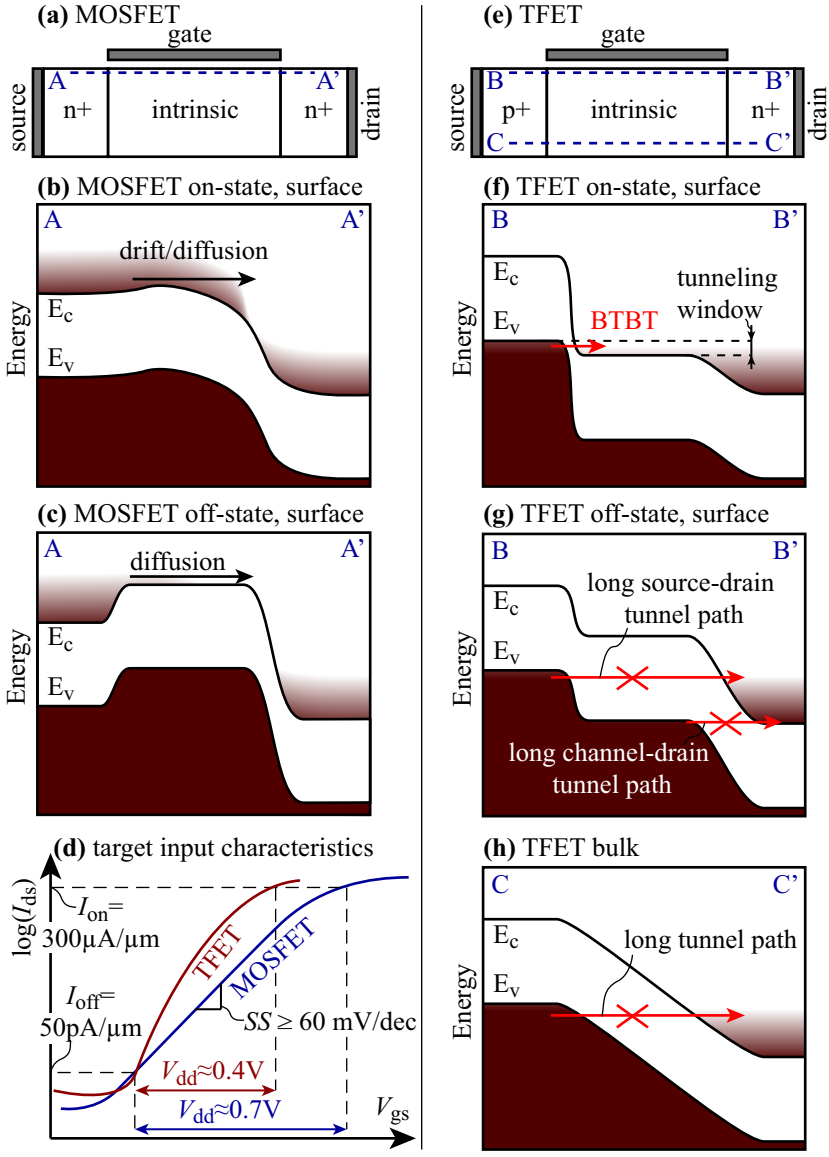


Figure 1.1: (a) shows the MOSFET cross-section, with A-A' surface band diagrams in (b) on-state and (c) off-state. Red shades indicate occupied electron states and white indicates empty states. (d) shows MOSFET transfer characteristics with $SS \geq 60$ mV/dec, and target characteristics of an optimized TFET operating at smaller V_{dd} than the MOSFET. The target I_{on}, I_{off}, V_{dd} metrics are proposed in section 1.3. (e) shows the TFET cross-section with the B-B' surface band diagrams in (f) on-state and (g) off-state. (h) shows the TFET C-C' bulk band diagram.

BTBT occurs from filled states in the p+ source (colored red) to empty states in the intrinsic region (white). The tunneling paths are very short, typically 3nm. In the ballistic regime, only carriers in the tunneling energy window are transmitted.

In the TFET off-state (figure 1.1(g)), the gate voltage is low and the energy bands near the gate move up . The tunnel paths are now much longer, typically >50 nm to obtain a sufficiently low I_{off} for $In_{0.53}Ga_{0.47}As$ TFET. Compared to a MOSFET, the high-energy carriers from the Fermi-Dirac tail are now eliminated by the bandgap in the p-type source, and thermionic emission is therefore absent. It is the abrupt change from short to long tunnel paths that causes a swing potentially <60 mV/dec. This steep swing allows TFETs to operate at potentially smaller V_{dd} and lower power than MOSFETs.

The TFET is an ambipolar device, which means current conduction by both electrons and holes are both possible. For the case of n-TFET, electrons tunnel from the source to the intrinsic region in the on-state, but holes can also tunnel from the drain to the intrinsic region in the off-state. Equivalently, this can be seen as electrons tunneling in the opposite direction, as shown by the arrow at the bottom-right side in figure 1.1(g). In order to suppress this parasitic tunneling in the off-state, a common solution is to use a much lower doping concentration at the drain than at the source. Figure 1.1(g) shows a low electric field at the intrinsic region/drain interface, and tunneling along these long paths is suppressed. Another solution, proposed by Verhulst *et al.* [5], is to use a shorter gate which does not extend to the drain. This also lowers the electric field at the drain side.

In the on-state, the TFET always has a lower current than a similar MOSFET. Both devices have the same channel region where carriers flow by drift-diffusion, but the TFET has an additional tunneling barrier limiting the electron flow. Therefore, TFETs are targeted to replace Low Power (LP) CMOS, which have a lower I_{on} than high power CMOS but much higher ratio $I_{\text{on}}/I_{\text{off}}$. TFETs have the additional potential benefit of operating at lower V_{dd}, and therefore a lower power consumption than LP CMOS.

1.3 Figures of merit

The energy-delay product is one of the most accurate figures of merit to compare the performance of different TFET and MOSFET circuits [4], but it is difficult to extract it experimentally. It requires a fully optimized circuit with low resistance interconnects and low parasitic capacitance. Today, most TFET research is

taking place at the device level. Therefore, the following device-related metrics are commonly used.

A first option is to compare I_{on} and I_{off} for a fixed V_{dd}. Approximate target values for TFETs to be competitive with LP CMOS are I_{on}=300 µA µm^{-1}, I_{off}=50 pA µm^{-1} and V_{dd} ≤0.5 V. These values are roughly based on reports from the International Technology Roadmap for Semiconductors (ITRS) [6] and simulations by Nikonov *et al.* [4]. In section 3.9, we compare calibrated TFET simulations to these target values.

I_{60} is another figure of merit when comparing different TFETs in literature. I_{60} is the highest current where the transfer characteristics exhibit a transition from sub- to super-60 mV/decade [7]. This metric is simple and useful because it captures information from both the swing and the on-current. It was introduced by Vandenberghe *et al.* [7] and is now widely used in the TFET community. As a rough guideline, I_{60}>10 µA µm^{-1} is required to be competitive with MOSFETs.

A third commonly used metric is SS_{min}, which is the minimum value of $dV_{gs}/d\log_{10}(I_{ds})$. Even though the concept of a subthreshold regime does not exist in a TFET, the metric SS_{min} is widely used in literature and we will also occasionally use it in this thesis. Compared to the other metrics, SS_{min} contains the least information about competitiveness with MOSFETs, but SS_{min}<60 mV/dec is often used as a convincing proof of the tunneling injection mechanism of a TFET.

1.4 Most common TFET configurations

The most common TFET configuration is the so-called point-TFET. The gate only overlaps the intrinsic region, as shown in 1.2(a). In this two-dimensional cross-section image, all tunneling is concentrated near one point, close to the intersection of source, intrinsic and oxide regions. The tunneling current does not scale with any dimension of the device, except the oxide thickness and the electrical width of the device, in the dimension perpendicular to the image.

In a different TFET configuration called the line-TFET, the gate stack overlaps only the source region, as shown in figure 1.2(b). Strong band bending and therefore band-to-band tunneling occurs in the source itself. The current scales with overlap length L_{gs}. The point- and line-tunneling names were first proposed by Wang *et al.* [8].

When the gate overlaps both the source, intrinsic and drain regions, as shown in figure 1.2(c), both tunneling components are present. However, the onset of point tunneling occurs at lower V_{gs} than the onset of line-tunneling, because

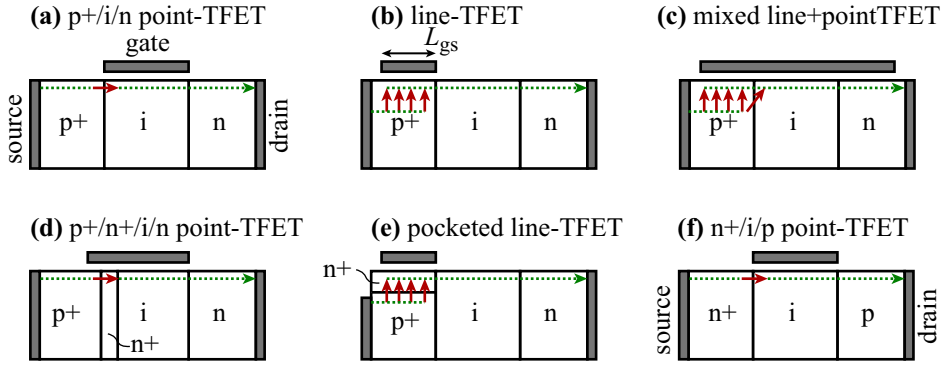


Figure 1.2: The most common TFET configurations are shown, with different gate positions and doped regions. In the on-state, the full red arrows indicate tunnel paths, and the dashed green arrows indicate carrier flow by drift/diffusion.

the potential in the undoped channel is modulated more easily by the gate voltage than the potential in the highly doped source. The drain overlap induces additional tunneling at the drain junction, but the resulting current is acceptable when the doping concentration in the drain is much lower than in the source. Although this is not the best TFET configuration, it is one of the easiest to fabricate, because the requirements for gate alignment are less stringent. Therefore, nearly all III-V point-TFETs in literature have a gate overlapping the source, channel and drain.

Figure 1.2(d) shows the addition of a counterdoped pocket, typically 3 nm thick, at the point-TFET source/intrinsic region interface. This creates a higher electric field resulting in higher I_{on}, and a more abrupt transition from short to long tunnel paths when decreasing V_{gs} [9, 10]. The same counterdoped pocket concept can also be applied to line-TFET (figure 1.2(e)) [11].

In the previous sections, only n-type TFETs are discussed. P-type TFET configurations are obtained by switching all dopant types, as shown in figure 1.2(f) for the point-TFET. In this case, holes tunnel from the conduction band in the source to the valence band in the intrinsic region.

Several configurations are discussed in the coming chapters of this thesis. Calibrated simulations of a pocketed n-type point-TFET and pocketed p- and n-type line-TFETs are performed in section 3.9. Also, line-TFETs and specifically the impact of field-induced quantum confinement is discussed in chapter 5. Finally, pulsed IV measurements are performed on p+/i/n point-TFETs in chapter 6.

1.5 Choice of materials for homo- and heterojunction TFETs

This thesis is focused on III-V compound semiconductors instead of the more common group IV semiconductors, because these are mostly direct bandgap semiconductors. They have the advantage of a higher BTBT rate, and therefore a higher TFET on-current. We will further elaborate on the BTBT rate in section 2.2.1.

The first material for which we calibrate BTBT is the ternary compound semiconductor $In_{0.53}Ga_{0.47}As$. We have chosen this material as a starting point because it is lattice matched to InP substrates, and high-quality epitaxial growth technology was already established at imec at the start of this thesis. Moreover, $In_{0.53}Ga_{0.47}As$ is also targeted as a channel material in imec's III-V MOSFET program, because it has a higher electron injection velocity compared to Silicon. Our research has therefore benefited from technological advancements in the III-V MOSFET program, mostly in terms of gate stack improvement but also characterization methods like Secondary Ion Mass Spectrometry (SIMS) and Capacitance-Voltage (C-V) measurements.

Materials with a smaller bandgap like InAs or InSb are beneficial to further boost the TFET on-current, but come with the penalty of higher off-current due to higher thermal generation of minority carriers and higher parasitic source-drain tunneling (shown in figure 1.1(g)). Furthermore, the smaller electron and hole effective masses in these materials lead to increased field-induced and size-induced quantum confinement in case of double gate or nanowire configurations. All these parasitic effects mask the intrinsic BTBT mechanism. Therefore we do not investigate these materials in this thesis.

It has been predicted that heterojunction TFETs with staggered or broken band alignments can achieve a better trade-off between high I_{on} and low I_{off} [12]. Therefore, the second set of materials we investigate is the $In_{0.53}Ga_{0.47}As/GaAs_{0.5}Sb_{0.5}$ heterojunction, which is lattice matched to InP substrates and has a staggered band alignment. Figure 1.3 schematically shows the band diagrams of a $In_{0.53}Ga_{0.47}As$ homojunction TFET, and a $In_{0.53}Ga_{0.47}As/GaAs_{0.5}Sb_{0.5}$ heterojunction TFET. For the latter, the conduction and valence band offsets at the source-channel junction lead to a smaller $E_{g,eff}$, shorter tunnel paths and therefore higher I_{on} than the homojunction TFET.

Another promising combination is the InAs/GaSb heterojunction, for which the broken gap alignment allows for a higher I_{on}. However for TFETs with a thick body, this also leads to a tunneling junction which is always open deep in

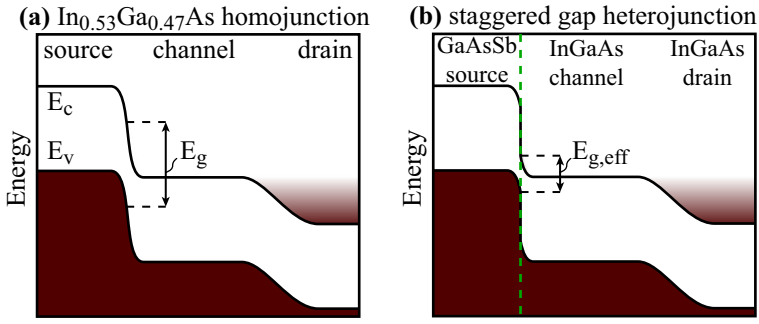


Figure 1.3: (a) shows a $In_{0.53}Ga_{0.47}As$ homojunction TFET, and (b) shows a staggered gap heterojunction TFET with shorter tunneling paths from $GaAs_{0.5}Sb_{0.5}$ source to $In_{0.53}Ga_{0.47}As$ intrinsic region.

the body where the gate has no electrostatic control. Avci *et al.* showed the InAs/GaSb heterojunction TFET is promising but only achieves sub-60mV/dec operation in a double gate or nanowire configuration with good electrostatic control (body thickness <5 nm) [13]. Since the technologies for high-quality epitaxial growth and nanowire etching of these materials were not yet mature at imec, this combination is not investigated.

1.6 Literature review of experimental III-V TFETs

In this section, we discuss the configuration, performance and challenges of experimental III-V homojunction and heterojunction TFETs which are relevant for this thesis. The first experimental III-V TFET was reported in 2009 by Mookerjea *et al.* from Penn. State University [14]. It is a pillar-based configuration, as sketched in figure 1.4(a). In the first step of the fabrication flow, a vertical stack of p+/100 nm i/n+ $In_{0.53}Ga_{0.47}As$ is grown by Molecular Beam Epitaxy (MBE). MBE allows epitaxial growth of heterostructures with sharp dopant transitions of only a few nm/dec. A $20\times11\mu m^2$ pillar is then chemically etched, and a gate stack is deposited on the sloped sidewall. The tunneling location is shown by the red arrow. The challenge in this fabrication flow is optimizing the wet etch and defect passivation processes to obtain pillar sidewalls with a low roughness and a low amount of semiconductor/oxide interface defects. These defects contribute to leakage by Shockley-Read-Hall (SRH) and Trap-Assisted Tunneling (TAT) generation [9].

In 2011 Dewey *et al.* from Intel took the same approach but included a strained

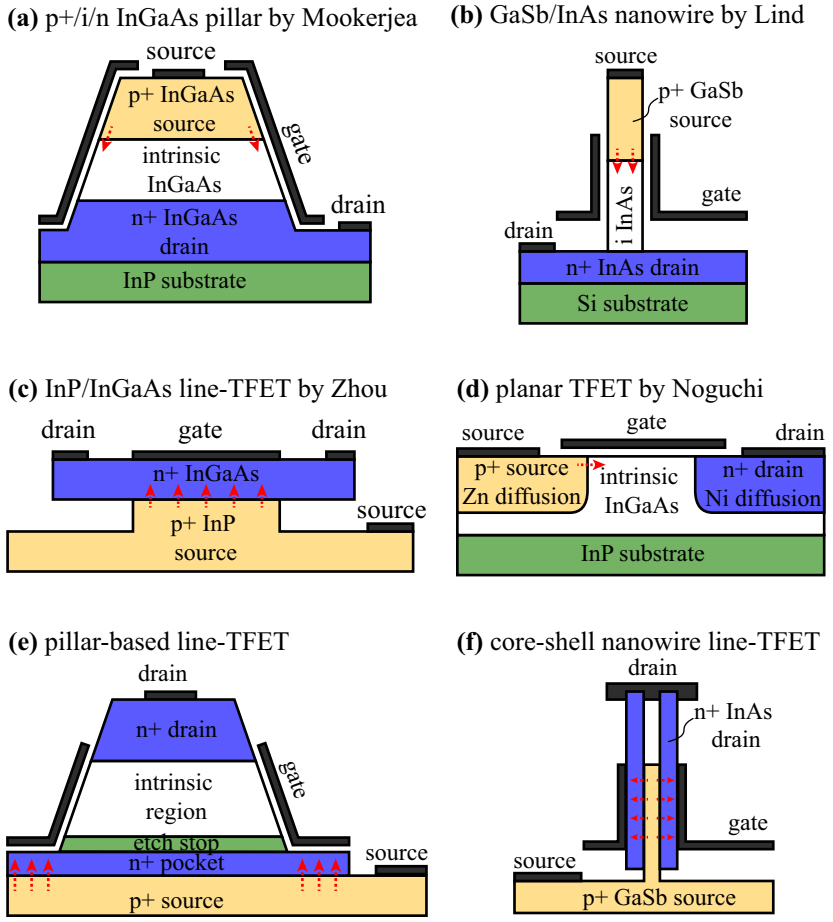


Figure 1.4: Experimental III-V TFETs in the literature inlude (a) pillar based point-TFET[14], (b) nanowire point-TFET [15], (c) underetched line-TFET [16], and (d) dopant diffusion based planar TFET [17]. We submitted patent applications for (e) a pillar-based line-TFET and (f) a core/shell nanowire line-TFET concept. The location of BTBT is shown by dashed arrows. Insulator regions are not shown.

6 nm $In_{0.70}Ga_{0.30}As$ pocket (with smaller bandgap) between source and channel, and reduced the Effective Oxide Thickness (EOT) from 4.5 to 1.1 nm. Compared to Mookerjea's device, this decreases SS_{min} from 190 mV/dec to 58 mV/dec, with I_{60}=3×10^{-3} µA µm^{-1}. Dewey's device is the first demonstration of sub-60 mV/dec operation in III-V TFETs.

One of the latest iterations of the pillar-based configuration was reported by Pandey *et al.* from Penn State University [18]. They use the following staggered gap heterojunctions to further boost I_{on}: p+/i/n $GaAs_{0.40}Sb_{0.60}/In_{0.65}Ga_{0.35}As$ for nTFET and n+/i/p $In_{0.7}Ga_{0.30}As/GaAs_{0.35}Sb_{0.65}$ for pTFET. They use a ZrO gate oxide with EOT 0.7 nm, and the pillar width is 700 nm. Compared to Dewey's device, the staggered gap heterojunction and thinner EOT boosts the nTFET I_{on} from 12 to 245 µA µm^{-1}, but also puts a penalty on SS_{min} (58 to 102 mV/dec). In chapter 6 we present pulsed *I-V* measurements of this nTFET, in an attempt to reduce SRH and TAT and hence I_{off}. These measurements were performed in a collaboration between the National Institute of Standards and Technolgy (NIST), Penn State University and imec.

Instead of etching a III-V semiconductor stack and depositing the gate stack on the sloped and defect rich sidewall, Zhou *et al.* from Notre Dame University presented a line-TFET made by a radically different approach [16]. As shown in figure 1.4(c), on top of a p+ InP source, they place a 15 nm n+$In_{0.53}Ga_{0.47}As$ layer followed by a patterned gate stack. The drain is formed by contacting the $In_{0.53}Ga_{0.47}As$ layer next to the gated region, and the ungated source-drain leakage path is removed by chemically under-etching the InP.

In 2013 Yu *et al.* from MIT used the same ingenious approach to make a $GaAs_{0.5}Sb_{0.5}/In_{0.53}Ga_{0.47}As$ line-TFET [19]. They demonstrated that the tunneling current scales with gate-channel overlap area, proving the line-TFET operation principle. In chapter 5 of this thesis, we will show that field-induced quantum confinement significantly impacts the performance of these TFETs.

In 2013 Dey *et al.* from Lund Univ. demonstrated a p+/n+ GaSb/InAs broken gap line-TFET in a nanowire configuration, grown by Metal-Organic Chemical Vapor Deposition (MOCVD) [20]. In 2015 Lind *et al.* from the same group presented a p+/i/n GaSb/InAs point-TFET [15], also in a nanowire configuration with 30 nm diameter, sketched in figure 1.4(b). Although these TFETs did not show the same performance as nanopillar-based alternatives, these nanowire TFETs belong to the most advanced and scalable III-V TFETs in literature.

In 2013 Noguchi *et al.* from Tokyo Univ. presented a new planar approach for homojunction $In_{0.53}Ga_{0.47}As$ TFETs, where Zinc dopant atoms are introduced in the source by thermally activated diffusion from a spin-on glass [17]

(figure 1.4(d)). It was reported that these diffused dopants might induce less defects and hence less TAT than in-situ doping. Our TFET team at imec took the same approach, but the source, channel and drain material are replaced by $In_{0.7}Ga_{0.3}As$ to boost I_{on}. Alian *et al.* presented the results in 2015 [21]. Fast *I-V* measurements of this homojunction TFET are also discussed in chapter 6.

1.7 Patented TFET fabrication flows

We propose two new line-TFET fabrication flows. The first design, patented in 2013 [22] and shown in figure 1.4(e), addresses the need for a III-V pocketed line-TFET fabrication flow. Kao *et al.* showed that the counter-doped pocket decreases field-induced quantum confinement while keeping a high I_{on} [23].

The first step of the fabrication flow consists of the MBE growth of the full semiconductor stack. A nano-pillar is then formed by chemically etching the drain and intrinsic region. This is followed by a selective etch of the etch stop layer, which reveals the counterdoped pocket region with low surface roughness. In the final steps, the gate stack and contacts are deposited on the counterdoped pocket and on the sloped sidewall. The end result is a line-TFET with an anticipated lower defect concentration near the tunneling region, critical for low I_{off}.

The second proposed line-TFET fabrication flow, shown in figure 1.4(f) addresses the need for a III-V line-TFET with a small wafer footprint. The main advantage of this concept is that the on-current scales with the nanowire height, and it doesn't require a larger footprint on the wafer like planar technology. Furthermore, it is a simple configuration with only two semiconductor regions.

In the first step, a p-type GaSb nanowire is grown on a patterned substrate by Metal-Organic Chemical Vapor Deposition (MOCVD), forming the TFET source. A n-type InAs shell is then grown around the nanowire by MOCVD. Then, the gate stack is deposited around the shell layer. The top part of the GaSb core is selectively removed by chemical etching, creating a void. Finally, the source and drain contacts are deposited. A line-TFET is obtained, where tunneling occurs radially from the GaSb source to the InAs shell.

A patent for the device configuration and the fabrication flow was filed in May 2013 [24]. In November 2013, Dey *et al.* from Lund University published experimental results of a very similar TFET [20], also a GaSb core/InAs shell nanowire line-TFET, but with a different drain isolation approach.

1.8 Goal of this thesis

Semi-classical and quantum mechanical simulations are crucial to identify promising III-V TFET configurations and guide the TFET fabrication. However, there is uncertainty on the accuracy of the relevant models and the input parameters. Therefore, the topic of this thesis is the experimental calibration of these models. We achieve this using tunnel diodes and MOS-CAP, which are simpler to fabricate and to characterize than complete TFETs. This allows us to decouple the different effects occurring in a TFET. We aim to identify the BTBT, SRH and TAT current components, the effects of bulk and interface traps, the effects of dopant- and temperature dependent bandgap narrowing and the energy band alignment of heterojunction TFET. In a final step, we attempt to measure the pure BTBT, 'intrinsic' TFET characteristics using cryogenic pulsed *I-V* measurements, to compare these to calibrated TFET simulations in future work.

1.9 Organization of this thesis

In chapter 2, we thoroughly discuss the operation principle of tunnel diodes for BTBT calibration. We cover the semi-classical and quantum mechanical simulators, the models and input parameters to predict the BTBT current in tunnel diodes and TFETs. We design tunnel diodes for BTBT calibration, and we motivate the choice of materials, doping profiles, and we set requirements for the diode dimensions to prevent excessive parasitic series resistance. In appendix C, we develop a new process flow for the fabrication of $In_{0.53}Ga_{0.47}As$ tunnel diodes that satisfy these dimensional requirements. All process steps are documented such that the flow can be replicated in imec's III-V clean room or in another lab.

In chapter 3, we identify the different generation/recombination mechanisms in these tunnel diodes using electrical measurements, and we calibrate the BTBT, SRH and TAT models. We then perform calibrated simulations of $In_{0.53}Ga_{0.47}As$ TFETs and investigate their competitiveness with Silicon MOSFET.

In chapter 4, we investigate the impact of the effective bandgap for heterojunction tunneling ($E_{g,eff}$) in the $GaAs_{0.5}Sb_{0.5}/In_{0.53}Ga_{0.47}As$ heterojunction. There is still significant uncertainty on this parameter, especially if we consider the impact of heavy doping of the TFET source and pocket at the tunnel junction. We demonstrate using quantum mechanical simulations how the uncertainty in $E_{g,eff}$ affects key performance metrics. We calibrate $E_{g,eff}$ using p+/i/n+ heterojunction tunnel diodes, for which tunneling occurs in the nearly intrinsic

region. We investigate the impact of heavy doping by also calibrating $E_{\mathrm{g,eff}}$ using p+/n+ heterojunction tunnel diodes, which are severely affected by dopant-dependent bandgap narrowing.

In chapter 5, we consider the impact of Field-Induced Quantum Confinement (FIQC) which occurs in all TFET, but this effect is not included in semi-classical simulations. We experimentally demonstrate that FIQC delays the onset of BTBT, as predicted by quantum mechanical simulations. We achieve this result using highly doped MOS-CAPs, for which we demonstrate AC inversion by BTBT.

In chapter 6, we investigate whether we can suppress parasitic oxide trap charging and parasitic SRH/TAT generation in TFETs by performing pulsed I-V (PIV) measurements. The goal is to gain additional insight in these non-idealities, and to investigate whether trapping-free transfer characteristics can be achieved with cryogenic PIV measurements.

Chapter 2

Modeling and design of tunnel diodes for BTBT calibration

When a tunnel diode (Esaki or Zener diode) is reverse biased, its band bending is similar to the on-state band bending of a point-TFET at the source-channel tunnel junction. Since tunnel diodes are easier to fabricate and characterize than TFETs, tunnel diodes are better for BTBT calibration. In the section 2.1, we introduce Esaki and Zener diodes more thoroughly, and we link their operation to the TFET. In section 2.2 we discuss the different models used to predict the current-voltage (I-V) characteristics of tunnel diodes and TFET. These include the semi-classical and quantum mechanical BTBT models, which we will calibrate in chapter 3. We then give an overview of other parasitic current contributions in Esaki diodes, and the methods to identify them. In section 2.4, we focus on the optimal design of tunnel diodes for BTBT calibration. We discuss the benefits of calibrating BTBT in forward or reverse bias, the use of p+/n+ or p+/i/n+ diodes, we determine the target dimensions and the different contacting schemes.

2.1 Esaki diodes and Zener diodes

2.1.1 Operation principle

Leo Esaki received the nobel prize in physics for his pioneering work on quantum mechanical tunneling of electrons [25]. In 1958 he observed an "anomalous current-voltage characteristic in the forward direction" in degenerately doped Germanium p-n diodes [26]. Degenerate doping occurs when the dopant concentrations are sufficiently high such that the electron quasi Fermi level (E_{fn}) in the n-type neutral region is located above the conduction band edge, and the hole quasi Fermi level (E_{fp}) in the p-type neutral region is located below the valence band edge, as shown in figure 2.1(d). This means the conduction band in the n+ region energetically overlaps with the valence band in the p+ region at zero bias. The bands are then 'crossed'. When a small positive or negative bias is applied, Band-to-Band Tunneling (BTBT) of electrons is possible from one region to the other.

The I-V characteristic of the so-called Esaki diode are shown in figure 2.1(f). In reverse bias ($V_{\mathrm{np}}>0$, figure 2.1(e)), electrons tunnel from filled states in the valence band of the p+ region to empty states in the conduction band of the n+ region. Semi-classically this is interpreted as BTBT generation (G_{BTBT}) of electron-hole pairs. At small forward bias (figure 2.1(c)), electrons tunnel from occupied states in the conduction band of the n+ region to empty states in the valence band of the p+ region, which is electron-hole pair recombination (negative G_{BTBT}). When the forward bias is further increased the bands no longer overlap, they become 'uncrossed' in figure 2.1(b) and the BTBT current drops to zero. This decrease in BTBT current at increasing forward bias is known as Negative Differential Resistance (NDR), and is the anomalous characteristic Esaki was referring to. When further increasing forward bias (figure 2.1(a)), thermal diffusion current dominates and the well-known exponential I-V relation of the diode is recovered.

A diode which has dominant BTBT only in reverse bias is commonly called a Zener diode [28]. This occurs when the Fermi levels are non-degenerate, caused by lower doping concentrations than in Esaki diodes. At zero bias, the bands of the Zener diode are uncrossed, and the tunneling energy window is closed. Only at larger reverse bias, BTBT occurs. We use the name *tunnel diode* to capture both Zener and Esaki diodes [29, p. 521].

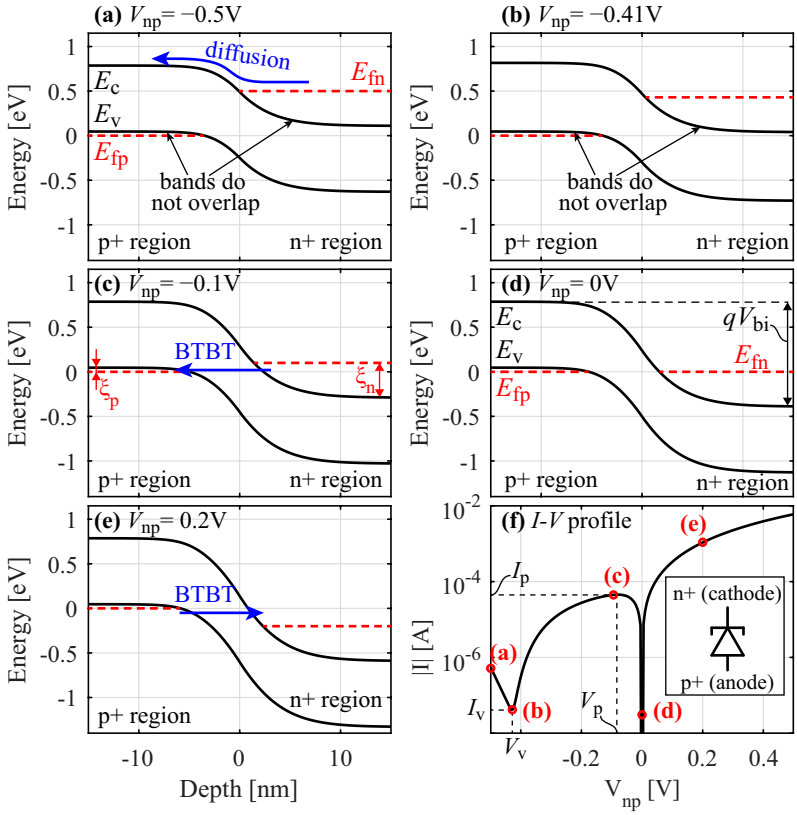


Figure 2.1: We perform Sentaurus Device simulations [27] of a p+/n+ $In_{0.53}Ga_{0.47}As$ Esaki diode with N_A=N_D=$2 \times 10^{19}\,cm^{-3}$ to show (a-e) the band bending at different applied bias and (f) the I-V profile with dominant BTBT current for V_{np}>-0.41 V and thermal diffusion current for V_{np}<-0.41 V. The inset in (f) shows the contacts to the p+ and n+ regions correspond to anode and cathode respectively.

2.1.2 Historic research interest and important metrics

From a historic point of view, the important performance metrics of Esaki diodes are the peak current I_p (figure 2.1(f)), the peak voltage V_p , the valley current I_v, the valley voltage V_v, and the Peak-To-Valley Current Ratio (PVCR=I_p/I_v). The early applications of Esaki diodes were oscillators in the microwave frequency regime, which exploit the NDR characteristic of Esaki diodes [30]. Therefore, there was a lot of interest in modeling I_p, I_v and increasing the PVCR through technological innovation. However, this field of applications was quickly overtaken by Resonant Interband Tunneling Diodes (RITD), which have a superior PVCR [30]. Currently, tunnel diodes are produced on a small scale for frequency converters [31], multijunction solar cells [32] and Static Random Access Memory (SRAM) applications [33].

2.1.3 More recent research interest linked to TFETs

There has been a revival in Esaki diode research with the emergence of the TFET, due to the similar operation principle of both devices. When a p+/i/n+ point-TFET (introduced in section 1.4) is biased in the on-state, the band bending near the source-channel interface (figure 1.1(f) on p. 9) is similar to the band bending in a reverse biased Esaki diode (figure 2.1(c,e) on p. 23). Researchers have compared the Esaki diode peak current I_p for different semiconductors and doping concentrations to guide TFET research [34, 35, 36], because I_p is roughly proportional to the TFET I_{on}. I_p in forward bias is often chosen as an unambiguous performance metric, because it is not impacted by a possible parasitic series resistance. The BTBT current at a chosen reverse bias can also be used as a metric, but the choice of bias is arbitrary and possibly inaccurate due to series resistance, which reduces the electrostatic potential drop at the tunnel junction.

In the TFET off-state, the bands are 'uncrossed' (figure 1.1(g) on p. 9), similar to the Esaki diode band bending in forward bias (figure 2.1(b) on p. 23). In this state, defect-assisted Shockley-Read-Hall (SRH) or Trap-Assisted Tunneling (TAT) leakage current is often dominant. Therefore, the PVCR is often used as a qualitative metric of the semiconductor quality [37, 38, 39, 40, 36, 41]. Also, when the TFET source is degenerately doped, the output characteristics show NDR for negative V_{ds}, which is commonly used to prove the TFET operation principle by BTBT [42, 43, 44, 15].

Zener diodes have a lower dopant concentration than Esaki diodes, and have dominant BTBT only in reverse bias. Recently, they have been used to calibrate BTBT in group IV materials [45, 46]. For III-V compound semiconductors

however, Zener diodes are less common because at doping concentrations typical for TFET (in the range 5×10^{18}-$1 \times 10^{20}\,\mathrm{cm}^{-3}$), the Fermi levels are degenerate due to the lower density of states of III-V materials, and Esaki behavior is obtained.

2.2 Modeling BTBT current in tunnel diodes and TFET

There are several ways to model the BTBT current in tunnel diodes and TFET. In section 2.2.1 we discuss the BTBT formalism by Keldysh and Kane, which gives intuitive understanding of the parameters important for BTBT: the effective masses, the density of states and the Fermi level positions, the bandgap and the energy band bending. In section 2.2.5 we then discuss how the Wentzel-Kramer-Brillouin (WKB) formalism is implemented for homojunction and heterojunction tunneling in the semi-classical simulator Sentaurus Device, and how it relates to the Kane formalism. Finally we introduce the implementation of the quantum mechanical BTBT simulator in section 2.2.6 . We will calibrate BTBT in chapter 3 for the semi-classical and the quantum mechanical simulators.

2.2.1 BTBT formalism by Keldysh and Kane

Most implementations of BTBT in semi-classical analytical models and simulators like Sentaurus Device are related to the formalism by Keldysh and Kane [47], where BTBT is modeled as generation/recombination of electron-hole pairs. If we consider a device made from a semiconductor with a direct bandgap E_g, a Temperature T=0 K and with a uniform electric field F in a volume V between the planes at $x = x_1$ and $x = x_2$ (figure 2.2), the BTBT generation rate G_BTBT of electron-hole pairs in units $\mathrm{s}^{-1}\,\mathrm{cm}^{-3}$ is given by

$$G_\mathrm{BTBT} = A_\mathrm{BTBT} \left(\frac{F}{F_0}\right)^2 \exp\left(\frac{-B_\mathrm{BTBT}}{F}\right) \tag{2.1}$$

where $F_0 = 1\,\mathrm{V/cm}$ and A_BTBT and B_BTBT are material-dependent input parameters:

$$A_\mathrm{BTBT} = \frac{g m_\mathrm{r}^{1/2} (qF_0)^2}{\pi h^2 \sqrt{E_\mathrm{g}}} \tag{2.2}$$

$$B_\mathrm{BTBT} = \frac{\pi^2 m_\mathrm{r}^{1/2} {E_\mathrm{g}}^{3/2}}{qh} \tag{2.3}$$

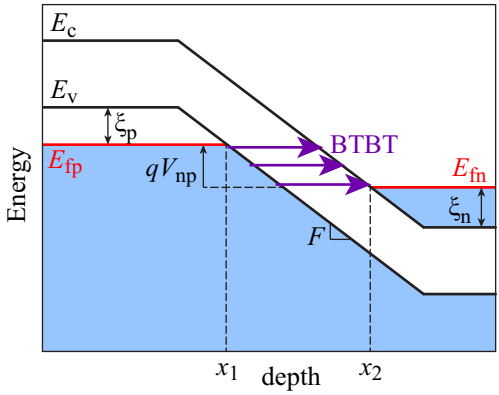


Figure 2.2: BTBT of electrons from filled states (shaded) in the valence band E_v to empty states (white) in the conduction band E_c, in a device a with uniform electric field F and T=0 K. ξ_n and ξ_p are the degeneracies of the Fermi levels in the n- and p-type neutral regions.

$$\text{with} \quad \frac{1}{m_r} = \frac{1}{m_c} + \frac{1}{m_v} \tag{2.4}$$

where g is the degeneracy factor and h is Planck's constant and q is the elementary charge. The reduced tunnel mass m_r is obtained from the conduction and valence band tunneling masses m_c, m_v, which are given by the electron effective mass m_e and light hole effective mass m_{lh}, respectively.

Using equations 2.2-2.3 and material parameters for different III-V semiconductors in references [48], we calculate the values in table 2.1 and plot G_{BTBT} in figure 2.3. G_{BTBT} has a negative inverse exponential dependence on F (equation 2.1). Therefore, BTBT typically only becomes important at high electric fields $F > 0.1\,\text{MV/cm}$. Materials like InAs with smaller E_g and smaller m_r have a higher BTBT rate and are therefore desirable for TFETs with high I_{on}.

The generation rate given by equation 2.1 is uniform in the volume V in the limit of $x_2 - x_1 \gg L_t$, where L_t is the tunnel path length given by $L_t = E_g/(qF)$. If we only consider BTBT in the volume V between the planes at $x = x_1$ and $x = x_2$, the total current is given by

$$I_{BTBT} = qVG_{BTBT} \tag{2.5}$$

Using equation 2.1 and figure 2.2, we can now identify important parameters for BTBT in Esaki diodes:

semiconductor	E_g[eV]	m_e [m_0]	m_{lh} [m_0]	A_{BTBT}[cm^{-3}s^{-1}]	B_{BTBT}[Vcm^{-1}]
InAs	0.35	0.023	0.026	1.7×10^{20}	1.3×10^{6}
$In_{0.53}Ga_{0.47}As$	0.74	0.043	0.052	1.6×10^{20}	5.6×10^{6}
$In_{0.73}Ga_{0.27}As$	0.56	0.033	0.041	1.6×10^{20}	3.2×10^{6}
$GaAs_{0.5}Sb_{0.5}$	0.77	0.045	0.066	1.7×10^{20}	6.3×10^{6}
InP	1.34	0.08	0.089	1.6×10^{20}	18×10^{6}

Table 2.1: BTBT parameters from the Kane formalism, calculated from parameters in reference [48]. E_g of $GaAs_{0.5}Sb_{0.5}$ is taken from reference [35].

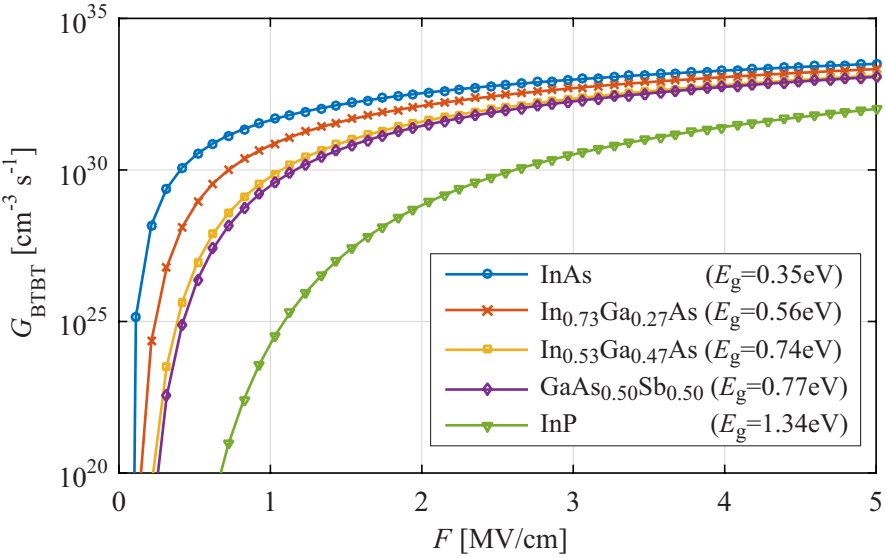


Figure 2.3: The generation rate for different direct bandgap III-V materials, calculated with equation 2.1 and the parameters in table 2.1.

- BTBT depends on the position of the electron and hole quasi Fermi levels in the neutral regions (E_{fn} and E_{fp}). These are discussed in section 2.2.2.
- BTBT depends on the bandgap E_{g}, which depends on the doping concentration and the temperature. These dependencies are modeled in sections 2.2.4 and 2.3.1.
- BTBT depends on the electric field F. Unlike in the device shown in figure 2.2, F is nonuniform in any real device, and the condition $x_2 - x_1 \gg L_{\mathrm{t}}$ does not hold. The BTBT rate then depends on the band bending, which can be approximated using the depletion approximation, or calculated self-consistently. Both models are compared in section 2.2.3. The semi-classical and quantum mechanical models consider the band bending accurately and are discussed in sections 2.2.5 and 2.2.6.

2.2.2 Density of states and Fermi level positions

The Fermi level positions in the neutral regions (figure 2.4) are calculated from the free hole (p) and electron (n) concentrations which are given by the acceptor and donor concentrations (N_{A} and N_{D}), the energy distribution of the available Density Of States (DOS) given by the electronic band structure, and the energy distribution of the occupation probability (Fermi-Dirac distribution). We first consider the case of non-degenerate doping: $\mathrm{n}<N_{\mathrm{c}}=2\times10^{17}\,\mathrm{cm}^{-3}$ and $\mathrm{p}<N_{\mathrm{v}}=8\times10^{18}\,\mathrm{cm}^{-3}$ [48] for $In_{0.53}Ga_{0.47}As$, where N_{c}, N_{v} are the conduction and valence band density of states. The DOS is approximated using a parabolic band structure $E=(\hbar k)^2/(2m^*)$ where $\hbar$ is the reduced Planck constant, k is the wavevector and m^* is the effective mass. The Fermi-Dirac (FD) electron distribution is approximated by the numerically faster Maxwell-Boltzmann (MB) distribution. In figure 2.4, we calculate the Fermi level positions for different hole and electron concentrations and extrapolate for degenerate dopant concentrations.

In case of degenerate doping concentrations, the previous model is inaccurate. We add three corrections to the model to obtain more accurate Fermi level positions. First, we include a nonparabolic band correction factor α to obtain the following dispersion relation: $E(1+\alpha E)=(\hbar k)^2/(2m^*)$ with $\alpha=1.35\,\mathrm{eV}^{-1}$ for $In_{0.53}Ga_{0.47}As$ [49]. Second, we consider a multivalley band structure by including the L, X satellite valleys in the conduction band and the split-off band in the valence band. Finally, the occupation probability is calculated using the Fermi-Dirac (FD) distribution. For doping concentrations typical in Esaki diodes $N_{\mathrm{A}}=N_{\mathrm{D}}=1\times10^{19}\,\mathrm{cm}^{-3}$, these three corrections have a large impact in case of n-type degenerate doping but a small impact for p-type degenerate doping (figure 2.4). However, using FD statistics instead of MB statistics increases the

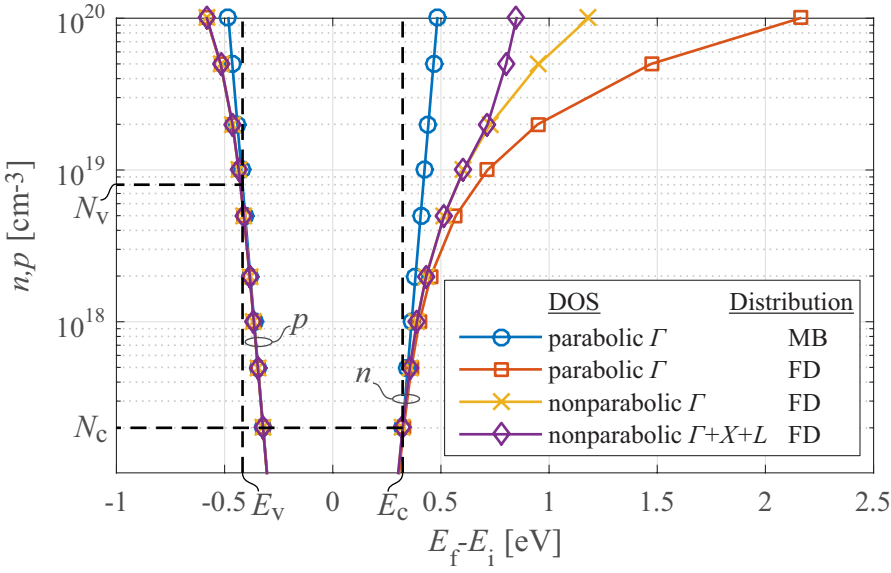


Figure 2.4: Calculation of Fermi level relative to intrinsic energy level $E_f - E_i$ in $In_{0.53}Ga_{0.47}As$ with different DOS models. The impact of dopant dependent bandgap narrowing (DOPBGN, section 2.2.4) is not included.

computational burden of a Sentaurus Device drift-diffusion simulation without BTBT by a factor ≈ 20. The Sentaurus Device commands for nonparabolic and multivalley band structure are shown in Appendix A,lines 46-47. The number of integration points for the numeric evaluation of the Fermi Dirac integral is set in line 126.

The Fermi level degeneracies $\xi_n = E_{fn} - E_c$ and $\xi_p = E_v - E_{fp}$ (figure 2.2) have a major impact on tunneling current in Esaki diodes through three separate effects. The first one is the electric field at zero bias, which is related to the built-in voltage $V_{bi} = (\xi_n + \xi_p + E_g)/q$ shown in figure 2.1(b). The second effect is the amount of filled/empty states to tunnel from/towards in forward bias, shown in figure 2.1(c). The third effect is the voltage at which the bands uncross (figure 2.1(d)) and the direct tunneling current drops to zero. Due to these three effects, the BTBT current is more sensitive to ξ_n, ξ_p in the NDR region than in reverse bias. This can be seen in figure 2.5, where ξ_n, ξ_p are calculated with the three different density of states models previously discussed, and the Esaki diode current is strongly dependent on the chosen model in forward bias but not in reverse bias. Due to the high sensitivity of the BTBT rate on the Fermi level positions, we will avoid calibrating BTBT in forward bias. We will further

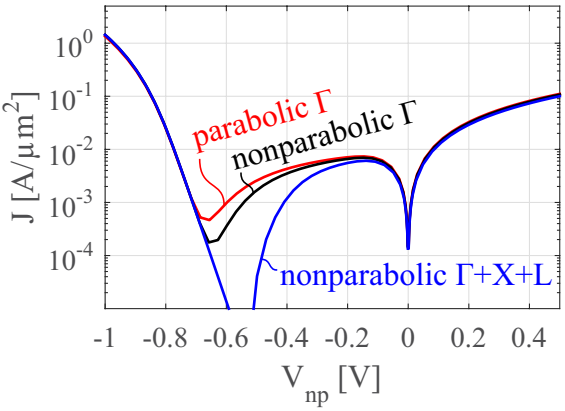


Figure 2.5: Esaki diode simulations show BTBT is impacted by the chosen DOS model and hence the position of the Fermi levels. The impact is large in the NDR region (forward bias) but small in reverse bias. Therefore we will avoid calibrating BTBT in forward bias. The BTBT current is calculated using the nonlocal dynamic tunneling model discussed in section 2.2.5.

discuss this in section 2.4.1.

2.2.3 Limits of the depletion approximation

The band bending in semiconductor devices is obtained from the Poisson equation, which in turn is obtained from the free carrier density, the doping concentrations and the applied voltages. When the semiconductor is depleted, e.g. in reverse biased diodes or depleted MOSCAP, we can obtain approximate analytic solutions by applying the depletion approximation, which assumes the free carrier concentration decreases abruptly to zero due to the band bending at the edge of the depletion region. This approach fails when the depletion region thickness is similar or shorter than the Debye length, the characteristic length scale for a change e in free carrier concentration. The Debye length is given by $L_\mathrm{D} = \sqrt{(\epsilon_s k_\mathrm{b} T)/(4\pi q^2 n)}$ for a non-degenerate semiconductor and $L_\mathrm{D} = \sqrt{(\epsilon_s \hbar^2 \pi^{1/3})/(4q^2 m^* 3^{1/3} n^{1/3})}$ for a degenerate semiconductor [50]. For a typical degenerate n-type dopant concentration $2 \times 10^{19}\,\mathrm{cm}^{-3}$ in our diodes in chapter 3, we obtain L_D=1.2 nm. This means the free carrier concentration cannot change by more than a factor e=2.7 over a distance of 1.2 nm.

In chapters 3 and 4, we will self-consistently calculate the band bending of strongly degenerate Esaki diodes, to get a accurate junction capacitances and

tunnel path lengths. In chapters 4 and 5, we will use the depletion approximation to obtain analytical solutions for the band bending in case of slightly degenerate p-type doping. We will verify and confirm the validity of these approximations.

2.2.4 Doping dependent bandgap narrowing and band tails

In literature, optical measurements have confirmed that heavy doping of semiconductors causes Doping-dependent Bandgap Narrowing (DOPBGN) and causes an exponentially decreasing density of states into the forbidden gap, also called band tails or Urbach tails [51]. These are caused by fluctuations in the electronic energy bands due to random dopant fluctuations and lattice vibrations [51, 52]. It has been predicted that band tails degrade the TFET subthreshold swing [53], and lead to a less steep NDR slope in Esaki diodes, where bands uncross [54]. In section 2.4.1 we will argue not to use the NDR region of the Esaki diodes for BTBT calibration, therefore we do not include the effects of band tails.

We include the effect of DOPBGN in Sentaurus Device using the Jain-Roulston model [55], which is based on physical material parameters and considers separate shifts of conduction and valence bands. The bandgap including DOPBGN is shown in Figure 2.6 as function of N_A and N_D and for different sets of Jain-Roulston parameters. For p-type doping, the parameters of Jain *et al.* [56] and Lopez-Gonzalez *et al.* [57] give consistent results. For n-type doping, the parameters from Jain *et al.* [56] appear to overestimate DOPBGN. For example, we obtain zero bandgap for $In_{0.53}Ga_{0.47}As$ with $N_D > 2 \times 10^{19}\,cm^{-3}$. Therefore we use the dataset from Cho *et al.* for $In_{0.53}Ga_{0.47}As$ [58]. For n-$GaAs_{0.5}Sb_{0.5}$, no DOPBGN parameters were found so we copy the parameters for n-$In_{0.53}Ga_{0.47}As$ since the parameters for p-$GaAs_{0.5}Sb_{0.5}$ and p-$In_{0.53}Ga_{0.47}As$ are very similar. The Sentaurus Device commands and parameters for DOPBGN are given in appendix A, lines 67, 210. Overall, we consider the uncertainty on DOPBGN quite high. Therefore we will avoid calibrating BTBT using devices where BTBT happens in highly doped regions affected by DOPBGN. This is further discussed in section 2.4.3.

2.2.5 Semi-classical implementations of the band-to-band tunneling process

The most accurate BTBT model in the semi-classical simulator Sentaurus Device is called the 'Nonlocal Dynamic BTBT model'. A first mesh point is taken as the start of a tunnel path (x=0). The tunneling energy is equal to the valence band energy $E_v(x=0)$ and the tunneling direction is the direction of the local electric

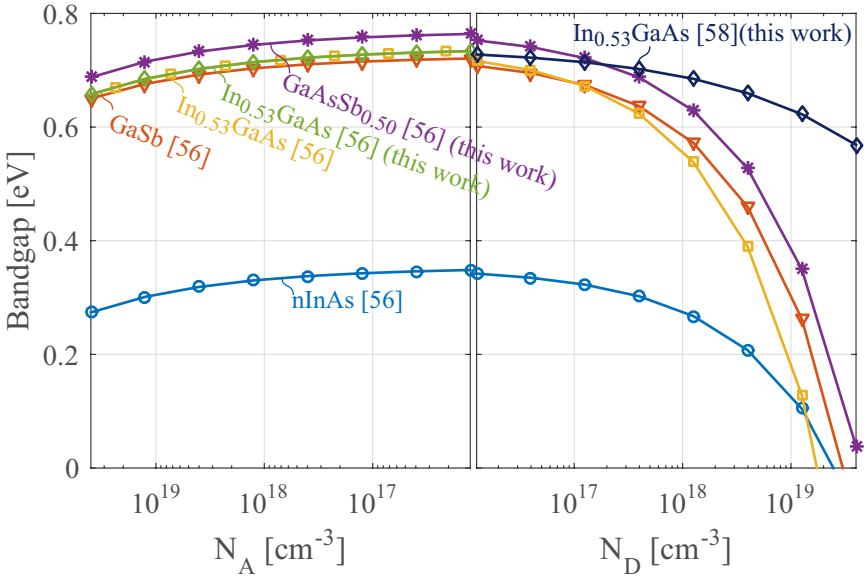


Figure 2.6: Calculation of the bandgap as function of doping, considering Jain-Roulston DOPBGN.

field. The end point of the tunnel path (x=L_t) is another mesh point where the conduction band has the same tunneling energy ($E_\mathrm{c}(x{=}L_\mathrm{t}){=}E_\mathrm{v}(x{=}0)$). The start and end points are shown by the arrow in figure 2.7(b), which shows a forward biased Esaki diode. The simulator then calculates the electron-hole pair generation rate G_BTBT according to equation (2.6) below. The holes are generated at the start of the tunnel path ($x = 0$), and electrons are generated at the end point (x=L_t). The simulator then repeats this procedure for every other mesh point. In the forward biased Esaki diode in figure 2.7(b), the Fermi-Dirac electron occupation probability is higher at the end of the tunnel path than at the start, therefore the generation rate is negative and we obtain electron-hole recombination.

G_BTBT is given by [59, equation (446)]:

$$G_\mathrm{BTBT} = |\nabla E_\mathrm{v}(0)| \times C_\mathrm{d} \times \exp\left(-2\int_0^{L_\mathrm{t}} \kappa dx\right) \times [\mathrm{FD_p}(0) - \mathrm{FD_n}(L_\mathrm{t})] \quad (2.6)$$

$$\mathrm{FD_p}(0) = \left(\exp\frac{E_\mathrm{v}(0) - E_\mathrm{fp}(0)}{k_\mathrm{B}T} + 1\right)^{-1} \quad (2.7)$$

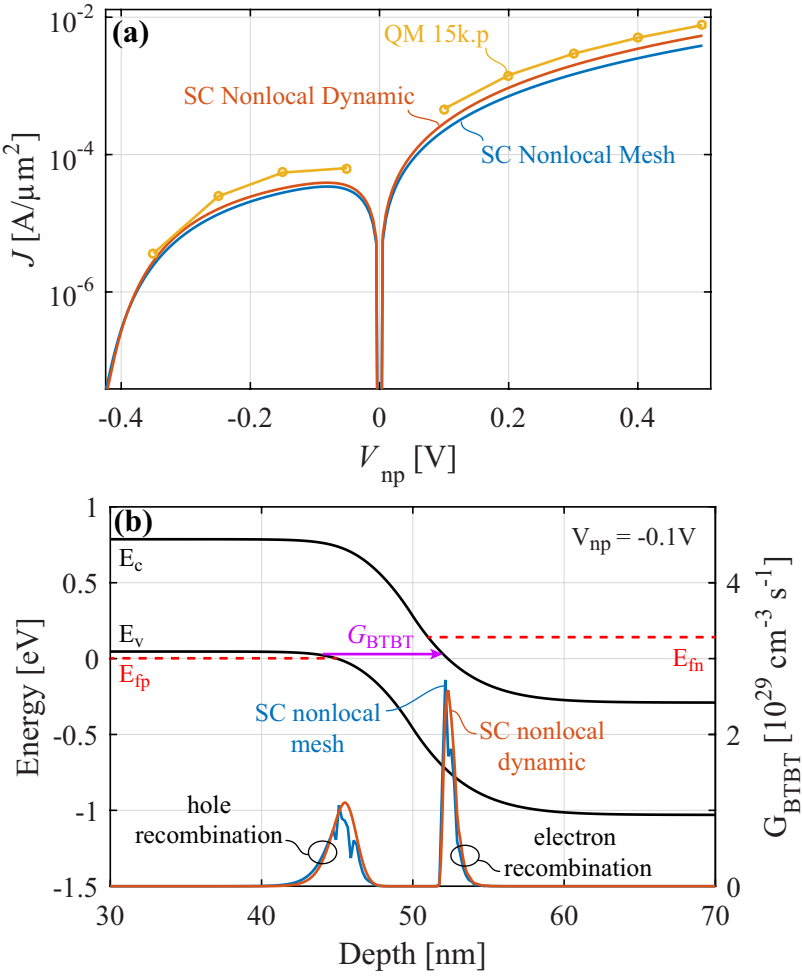


Figure 2.7: (a) Simulations of I-V characteristics of a p+/n+ $In_{0.53}Ga_{0.47}As$ diode at T=300 K and N_A=N_D=2×10^{19} cm^{-3}. Similar results are obtained for the two semiclassical (SC) implementations and the Quantum Mechanical (QM) BTBT model. (b) The corresponding band diagram and semi-classical BTBT rates shows nonlocal recombination of electrons and holes.

$$\mathrm{FD_n}(L) = \left(\exp\frac{E_\mathrm{c}(L) - E_\mathrm{fn}(L_\mathrm{t})}{k_\mathrm{B}T} + 1\right)^{-1} \tag{2.8}$$

where C_d is a prefactor accounting for the density of states, k_B is the Boltzmann constant and κ is the imaginary part of the wavevector in the forbidden gap. The exponential factor in equation 2.6 originates from the Wentzel-Kramer-Brillouin (WKB) approximation and represents the exponential damping of the electron wavefunction with increasing tunnel path length L_t. The position of E_fp and E_fn determine if there is BTBT generation $\mathrm{FD_p}(0) > \mathrm{FD_n}(L_\mathrm{t})$ or recombination $\mathrm{FD_p}(0) < \mathrm{FD_n}(L_\mathrm{t})$. In the uniform field limit and at T=0 K, equation 2.6 reduces to the Kane's BTBT equation (equation 2.1 on p. 25).

The term $\kappa(x)$ is obtained from the band bending $E(x)$ and the imaginary part of the dispersion relation $E(\kappa)$. The Kane, Franz and Keldysh dispersion relation models are supported in Sentaurus Device (Figure 2.8), and the Franz dispersion relation appears to be the most accurate, since it considers asymmetric electron-like and light hole-like branches and has a smooth transition between the two. In other work [60], it is shown that the Franz dispersion is a good approximation for the full-band dispersion for InAs, which is calculated with the OMEN simulator with a $\mathrm{sp^3d^5s^*}$ tight-binding approach. In case of heterojunction tunneling, G_BTBT is calculated in the same way, and $\kappa(x)$ is discontinuous at the hetero-interface [61].

There are two different implementations of the path search algorithm. The first one is the *nonlocal dynamic* model, in which "the tunnel path is determined dynamically based on the energy band profile" [27]. The dispersion relation is calculated from the parameters m_c, m_v which are either provided directly or calculated from the provided parameters A_BTBT, B_BTBT with equations 2.2-2.4. The second implementation is the *nonlocal mesh* model, and requires a nonlocal mesh predefined by the user. The model sweeps all points of the nonlocal mesh. It requires ≈10× more cpu time than the *nonlocal dynamic* model and accepts m_c, m_v as input parameters.

Both models give a similar result (figure 2.7(a)) when equivalent parameters are chosen with equations 2.2-2.4. Since the *nonlocal dynamic* model has a smaller computational burden and does not need a user-specified nonlocal mesh, we choose this model for semi-classical BTBT simulations. In previous work [34], the *nonlocal mesh* model was calibrated using Esaki p+/n+ diodes. This will be discussed in section 3.1.

Although the parameters A_BTBT, B_BTBT (or equivalently m_c, m_v) can be calculated from the theory by Keldysh and Kane (table 2.1), there is uncertainty whether the model provides sufficient accuracy. Therefore, we will calibrate the model for $\mathrm{In_{0.53}Ga_{0.47}As}$ in chapter 3, by comparing the measured and simulated BTBT current in Esaki diodes, and we will take A_BTBT and B_BTBT

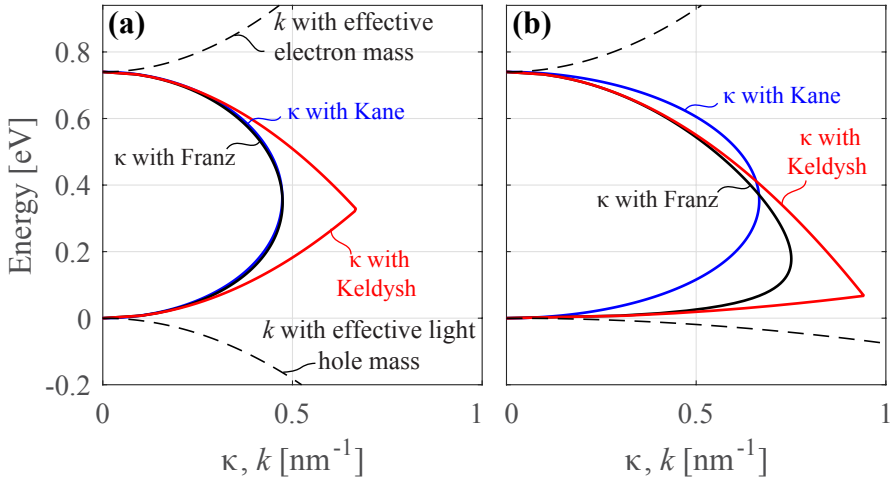


Figure 2.8: The real (k) and imaginary (κ) parts of the wavevector, calculated (a) for $In_{0.53}Ga_{0.47}As$ with $m_c = 0.043\,m_0$ and $m_v = 0.052\,m_0$, and (b) for a virtual material with $m_c = 0.05\,m_0$ and $m_v = 0.5\,m_0$. The Keldysh dispersion is calculated from [59, equations (458-459)], the Kane dispersion from [59, equation (448)] and the Franz dispersion from [59, equation (683)].

as fitting parameters. We will then compare our results to the theoretical values in table 2.1.

The Sentaurus Device commands and parameters for the *nonlocal dynamic* model are given in appendix A on lines 54, 193. The *nonlocal mesh* commands and parameters are shown on lines 49, 113, 205.

2.2.6 Quantum Mechanical BTBT implementation

The Quantum Mechanical (QM) simulator discussed in this thesis was developed and coded by Devin Verreck [62] and is based on the k·p envelope function formalism, applying quantum transmitting boundary conditions [63] at the contacts. The simulator supports tunneling through heterojunctions, and the difference in basis functions in the different materials is accounted for by transforming the momentum and Hamiltonian matrix elements.

The ballistic probability current is obtained by calculating the transmission probability through the barrier, multiplication with the Fermi-Dirac occupation probability at both sides, and integration over the energy and the perpendicular

momentum. The transmission probability depends on the band structure, which is computed with either a two-band or fifteen-band implementation. The input parameters are interband momentum matrix elements $\mathbf{P}_{\mathrm{i}}$ which indicate the coupling between the different bands. In a two-band implementation, the single input parameter $\mathbf{P}$ is a measure for the coupling strength between the conduction and the valence bands, and is usually listed in units of energy as E_{P} [64]:

$$E_{\mathrm{P}} = \frac{8\pi^2 m_0}{h^2}\mathbf{P}^2. \tag{2.9}$$

E_{P} can be derived from B_{BTBT} with the relation

$$B_{\mathrm{BTBT}} = \frac{\pi^2 E_g^2 m_0}{2h\sqrt{E_{\mathrm{p}} m_0/2}} \tag{2.10}$$

derived from calculations by Kane [47].

In figure 2.7(a), the BTBT current calculated using the 15-band QM simulator and the same energy band profile and quasi Fermi levels as in figure 2.7(b) is shown. There is a satisfactory match with the semi-classical nonlocal BTBT models, confirming the validity of the latter for the $In_{0.53}Ga_{0.47}As$ p+/n+ Esaki diode simulations. There is a factor 1.6 difference between the QM simulations and the semi-classical *nonlocal dynamic*, caused by the calibration of E_{P} using a 2-band implementation with a light hole instead of heavy hole effective mass approximation in the transverse direction. This is further discussed in section 3.6.

2.2.7 Limits of the semi-classical BTBT models

There are however specific situations in which the semi-classical models are no longer accurate, and the QM simulator must be used. First, if size quantum confinement occurs the band structure will be modified, resulting in higher E_{g}, lower DOS and lower I_{BTBT}. For $In_{0.53}Ga_{0.47}As$, our simulations show size confinement is expected to occur when one of the device dimensions is smaller than 10-15 nm.

Second, Field Induced Quantum Confinement (FIQC) can be induced by a strong electric field at a heterojunction with a conduction or valence band offset, such that a triangular-like potential well is formed in the semiconductor. This causes quantized energy levels in the conduction or valence band [65]. The heterojunction can be the semiconductor/gate oxide junction in a TFET, and FIQC will occur in all TFET configurations where the tunneling direction is at least partially oriented towards the gate stack. This type of FIQC will be

experimentally demonstrated in chapter 5. The heterojunction can also be a semiconductor-semiconductor heterojunction with a large band offset, such as in a n-$GaAs_{0.5}Sb_{0.5}$/p-$In_{0.53}Ga_{0.47}As$ diode or in resonant interband tunneling diodes [66]. However, BTBT to/from regions with this second type of FIQC is not encountered in this thesis.

Third, it has been shown in the past that the WKB approximation is accurate for electric fields $0<F<2\,\mathrm{MV/cm}$, but underestimates BTBT for larger $2\,\mathrm{MV/cm}<F<20\,\mathrm{MV/cm}$ and overestimates BTBT at even larger $F>20\,\mathrm{MV/cm}$ where reflections occur [67]. Furthermore, WKB does not consider reflections in heterojunctions with staggered band alignment [68] and broken band alignment like InAs/GaSb [69]. For the latter, the WKB approximation could overestimate the BTBT current by a factor 3 [69].

Fourth, the current implementation of the semi-classical BTBT model makes use of the effective mass approximation for the calculation of the density of states factor C_d in equation 2.6. This could give incorrect results for materials with strongly non-parabolic bands like InAs or InSb.

Finally, it has been reported that the WKB approximation fails when the tunneling window is small and in the NDR region of Esaki diodes [67, 70], which leads to overestimation of J_p and NDR steepness. However, we do not observe this discrepancy when comparing semiclassical and quantum mechanical simulations in figure 2.7(a).

In summary, to remain in the validity range of the semi-classical BTBT model, we will choose diode diameter larger than 15 nm in section 2.4.6 to prevent size-induced quantum confinement. In section 3.5.2, the calibration will be performed at electric fields lower than 2 MV/cm, for which the WKB approximation is sufficiently accurate. Field-induced quantum confinement does not occur in homojunction and $GaAs_{0.5}Sb_{0.5}$/$In_{0.53}Ga_{0.47}As$ diodes. Figure 2.7(a) shows the semi-classical simulator predicts similar p+/n+ $In_{0.53}Ga_{0.47}As$ Esaki diode characteristics as the quantum mechanical simulation. Therefore we conclude that the semi-classical model provides sufficient accuracy to perform BTBT calibration.

2.3 Identifying different current contributions in Esaki diodes

Besides BTBT, Esaki diodes have other parasitic current contributions: phonon-assisted BTBT, thermal diffusion current, SRH and TAT generation/recombination. These mechanisms lead to electron-hole pair generation in

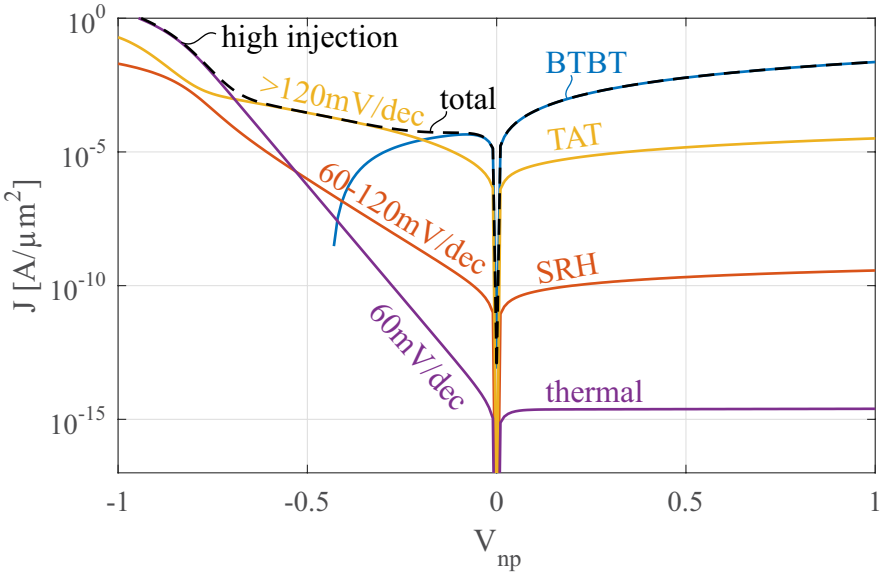


Figure 2.9: For a p+/n+ $In_{0.53}Ga_{0.47}As$ Esaki diode with $N_A{=}N_D{=}2\times10^{19}\,cm^{-3}$, we simulate the different current contributions using Sentaurus Device [27]. The SRH and Schenk TAT models have a minority carrier lifetime $\tau{=}1\times10^{-12}\,s$.

reverse bias, and recombination in forward bias. All contributions are shown in figure 2.9. In this section we describe methods to identify these current mechanisms, and avoid an incorrect BTBT calibration. These methods are similar for a TFET, where only the generation mechanisms occur, because in essence the TFET is a reverse biased diode where the band bending is applied by the gate voltage.

2.3.1 Direct BTBT

Temperature dependent *I-V* measurements are one of the most important tools to identify BTBT, because it is the only mechanism which is nearly temperature-independent in forward and reverse bias. Other parasitic current contributions like thermal diffusion current, SRH and TAT have a stronger temperature dependence, and are discussed in sections 2.3.5-2.3.6. We identify five effects that contribute to the small temperature dependence of BTBT in Esaki diodes:

1. The first and most significant effect is Temperature-dependent Bandgap Narrowing (TBGN). Figure 2.10 shows the bandgap of $In_{0.53}Ga_{0.47}As$ decreases with increasing temperature [71]. In turn, this causes increasing BTBT with increasing temperature.

2. The resulting smaller bandgap decreases the built-in voltage of the diode (V_{bi} shown in figure 2.1(b) on p. 23) and therefore decreases the electric field. This effect decreases the BTBT rate.

3. An increase in temperature causes a higher intrinsic carrier density and therefore a less degenerate Fermi level, as shown in figure 2.10 for p+$In_{0.53}Ga_{0.47}As$. The Fermi level shift can even cause the semiconductor to become non-degenerate at high temperature, and change the Esaki diode into a Zener diode.

4. An increase in temperature causes the Fermi-Dirac electron occupation to decrease more gradually with increasing energy. This effect is stronger in forward biased Esaki diodes, and will be further discussed in section 4.3.1.

5. For samples with a low dopant concentration, dopant atoms freeze out at cryogenic temperature. This decreases the free carrier concentration, decreases the electric field and decreases the BTBT current. However, we did not observe this effect in our degenerately doped $In_{0.53}Ga_{0.47}As$ and $GaAs_{0.5}Sb_{0.5}$ samples at T=4 K.

Due to these different effects, the BTBT rate either increases or decreases with increasing temperature. This dependence changes with the electric field, and whether the diode is in forward bias or reverse bias. BTBT does not follow an Arrhenius law ($I \propto \exp(-E_A/(k_B T))$ with k_B is the Boltzmann constant), but it is often convenient to extract the low activation energy E_A of BTBT to differentiate it from the higher activation energy of the SRH (section 2.3.5) and TAT (section 2.3.6) processes, discussed below. In literature, E_A=1.8 mV was extracted for the peak current of $In_{0.53}Ga_{0.47}As$ Esaki p+/n+ diodes [72]. We perform simulations using Sentaurus Device of the same device, while considering the five previously mentioned effects, and we extract a peak current activation energy of 8 meV near room temperature. In section 4.2.4 we will consider a model for the temperature dependence of the BTBT current, more accurate than the Arrhenius model, but only valid in p+/i/n+ diodes with low electric field.

The Sentaurus Device parameters for TBGN are given in Appendix A, lines 44,156,157.

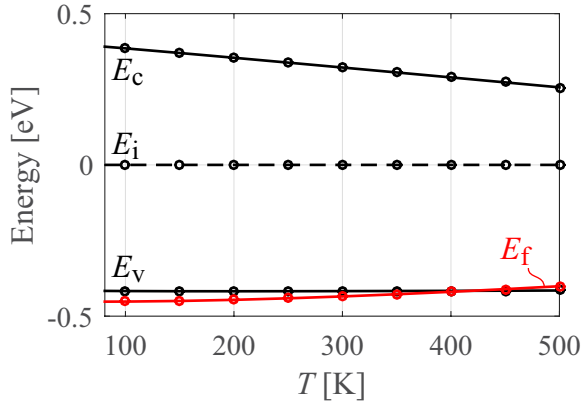


Figure 2.10: Calculation of E_f, E_c and E_v as function of temperature, calculated with Sentaurus Device for $In_{0.53}Ga_{0.47}As$ with N_A=1 × 10^{19} cm^{-3}. We consider a multivalley band structure, FD statistics and TBGN [71]. E_f becomes non-degenerate for T>400 K.

2.3.2 Phonon-assisted BTBT

Although little is known on phonon-assisted BTBT (or indirect BTBT) in direct-bandgap III-V semiconductors, it is expected to have the same profile as the direct BTBT I-V (figure 2.9), but with a smaller current value. However, it is possible that phonon-assisted BTBT is higher than direct BTBT in the valley region of the I-V, where the bands uncross and tunneling of electrons is only possible with a change in energy $\pm n_p \hbar \omega_p$ where n_p is the number of phonons and ω_p is the phonon angular frequency. Since we do not calibrate BTBT in this region of the I-V, we do not expect phonon-assisted BTBT to be an observable problem.

2.3.3 Thermal diffusion current

In forward bias, some electrons in the conduction band at the n+ side have sufficient energy to overcome the energy barrier and diffuse to the p+ region as minority carriers (figure 2.1(e)). They either diffuse to the metal contact or they recombine with the large amount of holes in the p+ region. The same process happens with holes at the n+ side. This thermal current can be recognized easily because it increases exponentially with forward bias (lower energy barrier) with an inverse slope equal to 60 mV/dec at room temperature (figure 2.9). It

has a positive temperature dependence with an activation energy E_a=E_g. At large forward bias (V_{pn}>0.4 V in figure 2.9 on p. 38), it typically becomes larger than the BTBT current. The thermal current can be suppressed by adding an additional energy barrier in the path of the diffusing minority carrier, like a heterojunction (section 2.4.5).

2.3.4 High injection

At even larger forward bias (V_{pn}>0.8 V in figure 2.9), the minority carrier concentration at the edge of the depletion region becomes comparable to the majority carrier concentration. The current then increases with forward bias with an inverse slope >60 mV/dec at room temperature (figure 2.9).

2.3.5 Shockley-Read-Hall (SRH) generation/recombination

In a reverse biased diode, the concentration of electrons and holes in the depletion region is lower than the thermal equilibrium concentration ($p \times n < n_i^2$, with n_i the intrinsic concentration). In the presence of defect states with an energy level E_t inside the bandgap, there is an enhanced generation of electron-hole pairs by the Shockley-Read-Hall (SRH) process. In a first step, a bound electron in the valence band is thermally excited to the trap energy level E_t, leaving a free hole in the valence band. In a second step, the trapped electron is thermally excited to the conduction band. The free electron (hole) then flows to the contact with positive (negative) bias by drift/diffusion. SRH current increases slightly with increasing reverse bias, mainly due to the larger depleted volume where $p \times n < n_i^2$.

In a forward biased diode with defect states, $p \times n > n_i^2$ and SRH recombination occurs. The defect acts as an efficient recombination center for electrons and holes. SRH recombination increases exponentially with increasing forward bias, due to the exponentially higher $p \times n$ product in the depletion region. In the log-lin plot in figure 2.9, SRH has an inverse slope between 60 mV/dec and 120 mV/dec [73, 74].

SRH generation/recombination is most efficient when the defect trap energy level E_t is located in the middle of the bandgap. In this case, SRH current can be recognized by its temperature dependence with activation energy E_a=E_g/2 [75].

In a n-type TFET with positive V_{ds}, SRH generation of electron-hole pairs occurs. It has been shown in literature that SRH contributes to the TFET off-state current [76, 21], but it is still unclear which type of defects contribute

to SRH leakage, and what the minority carrier lifetime is. In section 3.3.4 we will identify SRH by perimeter defects or by semiconductor bulk defects using $In_{0.53}Ga_{0.47}As$ Esaki diodes with different junction diameters. In section 3.7 we will calibrate the bulk SRH model using the $In_{0.53}Ga_{0.47}As$ diodes and apply this to $In_{0.53}Ga_{0.47}As$ TFET simulations since the semiconductor defects are identical in both devices.

2.3.6 Trap-Assisted Tunneling (TAT)

TAT generation/recombination, also called field-enhanced SRH, can be viewed semi-classically as a combination of electron tunneling to a defect state and a thermal excitation or relaxation. Due to the tunneling component, it is only dominant in diodes where the electric field is high, like the Esaki diode in figure 2.9.

In forward bias, TAT has an exponential I-V characteristic similar to SRH, but with a less steep slope [74]. TAT recombination is nearly temperature independent [77]. We experimentally confirm this in section 3.3.3, and we attribute this to the high electron and hole densities at the start and end of the tunnel path, which are nearly constant with temperature. Also, for TAT recombination, the electrons relax to a lower energy level, and this process does not require thermal energy.

In case of TAT generation in reverse bias, electrons are excited to a higher energy level. Therefore TAT generation increases with temperature with typically $0.1\,\text{eV} < E_\text{A} < E_\text{g}/2$ [75, 73]. TAT current originates from defects at or near the p/n junction, either in the semiconductor (area contribution) or at the diode sidewall (perimeter contribution).

In section 3.8, we will identify TAT recombination caused by bulk semiconductor defects from diode-size-dependent and temperature-dependent I-V measurements. We will calibrate the Sentaurus device's nonlocal TAT model and make predictions for the parasitic TAT generation in a point-TFET in section 3.9.1.

2.4 Design of tunnel diodes for BTBT calibration

We start by discussing the benefits of calibrating BTBT in forward versus reverse bias in section 2.4.1 and using p+/i/n+ versus p+/n+ diodes in section 2.4.3. Since the MBE growth and Esaki diode fabrication is done at imec, we have the freedom to choose the dopant profiles and the diode dimensions such that the BTBT models can be calibrated over a wide range of electric fields. However, if

we choose these such that the BTBT current contribution is too low, parasitic currents will mask the BTBT current. If on the other hand the total current is too high, the I-V characteristics will be distorted due to a potential drop over the parasitic series resistance. The choice of dopant profiles is discussed in section 2.4.4. The impact of series resistance and the choice of dimensions are discussed in sections 2.4.5-2.4.6.

2.4.1 Calibration in forward versus reverse bias

Calibration of BTBT models can be performed using the forward bias or reverse bias BTBT current of Esaki diodes. In figure 2.5 on p. 30 we have shown that the BTBT current is more sensitive to the Fermi level positions in forward bias than in reverse bias. The Fermi level positions determine the tunneling energy window, which is smaller in forward bias. Therefore, if the chosen multivalley model with nonparabolic correction (section 2.2.2) is not sufficiently accurate, a large error will be made when calibrating BTBT. In reverse bias, the tunneling window is larger and the BTBT current is less sensitive to the chosen DOS model (figure 2.5).

2.4.2 Calibration with Esaki versus Zener diodes

We argue that Esaki diodes are more useful than Zener diodes for BTBT calibration. First, when III-V materials are used with doping concentrations similarly high as in a TFET, Esaki diodes are usually obtained. III-V materials have a lower density of states than Silicon and Germanium and are therefore degenerately doped at doping concentrations typical for TFET.

Second, Esaki diodes have the additional peak current I_{p} and peak voltage V_{p} reference point. If the I-V profile of the diode is affected by a parasitic series resistance, V_{p} shifts to higher values due to the voltage loss over the series resistance, but I_{p} remains the same. This will be shown using a simple model in figure 2.14, and experimentally in section 4.3.3. V_{p} is therefore useful to characterize the series resistance.

If the parasitic resistance is very large, the electrostatic potential at the tunnel junction is possibly nonuniform due to a spreading resistance component. Therefore, we fabricate diodes with different diameters, and we verify whether the peak current density (J_{p}) is constant for all diodes. We use this method in appendix B to experimentally confirm a non-uniform potential in diodes with diameters $>100\,\mu\mathrm{m}$.

2.4.3 Calibration with p+/i/n+ versus p+/n+ diodes

In previous work where III-V Esaki diodes are benchmarked [78] and BTBT is calibrated [34, 58], p+/i/n+ with a thin 3 nm intrinsic region are targeted instead of p+/n+ diodes. This was chosen because at the junction, the p- and n-type dopant profiles have unintentional dopant slopes of a few nm/dec. The thin 3 nm 'intrinsic' region is therefore unintentionally doped, but it helps separating both dopant species and avoid counter-doping. Furthermore, our simulations show that the peak current density J_p is higher in $In_{0.53}Ga_{0.47}As$ p+/3 nm i/n+ compared to $In_{0.53}Ga_{0.47}As$ p+/n+ diodes. This is counter-intuitive, because p+/3 nm i/n+ diodes have a lower maximum electric field. This effect is caused by the highly asymmetric $\xi_n \gg \xi_p$ in $In_{0.53}Ga_{0.47}As$ (figure 2.4 on p. 29). By adding the thin intrinsic layer, the electric field in the tunneling region is more uniform and the tunneling energy window aligns better with the maximum overlapping density of states (plot not shown).

For the BTBT calibration purpose in this thesis, we prefer p+/i/n+ diodes with an intrinsic region longer than 3 nm for two different reasons. First, the intrinsic region is nearly depleted of carriers, and it covers nearly the whole electrostatic potential drop. The energy band bending is approximately linear in the intrinsic region and negligible in the p+ and n+ regions. Therefore, the electrostatic potential profile is less sensitive to unintentionally sloped dopant profiles, which are difficult to measure accurately. Secondly, all BTBT happens in the intrinsic region of the p+/i/n+ diodes, which is less affected by DOPBGN (introduced in section 2.2.4). This mitigates the uncertainty about the DOPBGN model and parameters, which results in a more accurate BTBT calibration.

When the intrinsic region is longer than 100 nm, the electric field is so low (F<0.1 MV/cm at zero bias) that BTBT is negligible. These diodes are typically used in photodetectors with low parasitic leakage current ("dark current") in reverse bias [79, 80, 81, 82]. For our purpose of BTBT calibration, we wish to suppress parasitic TAT and SRH contributions, and some fabrication and defect passivation techniques in appendix C is inspired by the previously mentioned references.

2.4.4 Choice of semiconductors and target dopant concentrations

The semiconductor for which we calibrate the BTBT models is $In_{0.53}Ga_{0.47}As$. It is chosen because it can be grown epitaxially with Molecular Beam Epitaxy (MBE) with high quality on lattice matched InP substrates, and the imec TFET program also primarily focuses on $In_{0.53}Ga_{0.47}As$. The p+ and n+ target doping concentrations for p+/i/n+ diodes are chosen sufficiently high

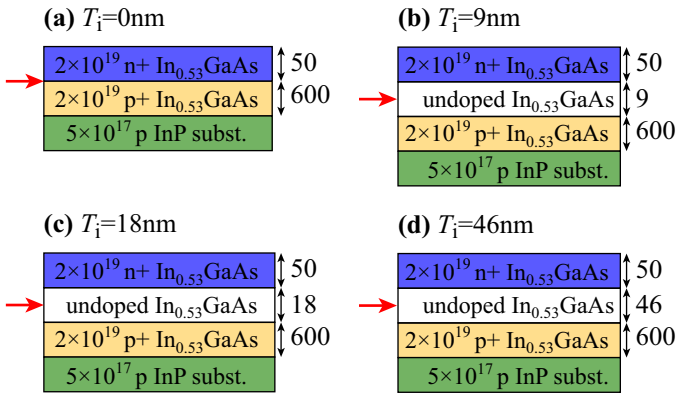


Figure 2.11: The different target stacks. All dimensions are in nanometers. The red arrow indicates the region where BTBT occurs, which we call the tunnel junction.

(N_A=N_D=2 × 10^{19} cm^{-3}) compared to the background impurity concentration in MBE (≈1 × 10^{16} cm^{-3}) in order to obtain the desired uniform electric field. Furthermore, these dopant concentrations are sufficiently high such that the NDR characteristic in forward bias is present.

In appendix C, we fabricate diodes with three different target intrinsic region thicknesses T_i to cover a wide range of electric fields. Given the restriction 3 nm<T_i<100 nm in the previous paragraph, we choose T_i=9, 18, 46 nm. These 'intrinsic' regions are actually unintentionally doped, but we use the word 'intrinsic' because it is widely used in this scientific field. For comparison with other work in literature, we also include a p+/n+ stack, which we label T_i=0 nm. The target stacks are shown in figure 2.11. We choose 50 nm for the top n+ layer thickness, which is sufficiently long for easy contact fabrication, and sufficiently short to prevent series resistance. The choice of 600 nm p+ layer thickness is also related to series resistance, and discussed in section 2.4.6.

In chapter 4 we will experimentally extract the band alignment of the $GaAs_{0.5}Sb_{0.5}$/ $In_{0.53}Ga_{0.47}As$ heterojunction. We will also fabricate Esaki diodes with those materials, and the choice of stacks will be discussed in chapter 4.

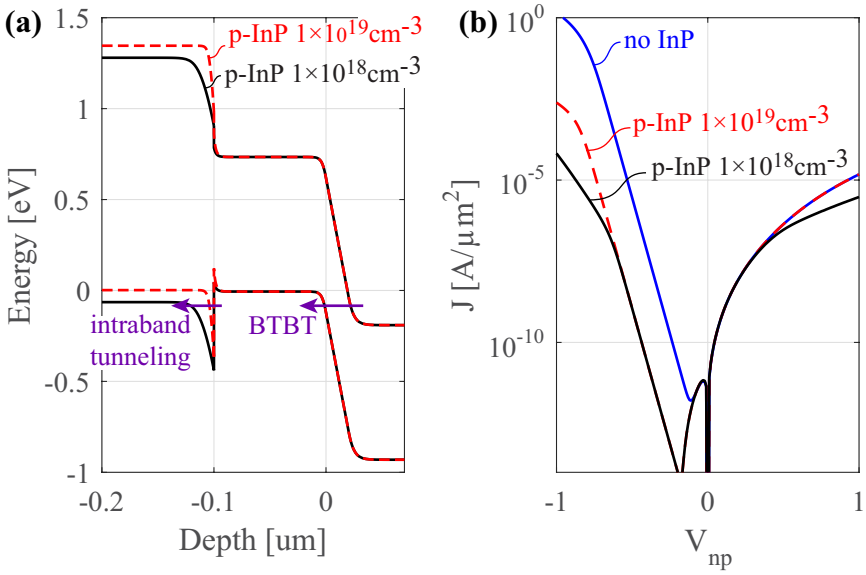


Figure 2.12: Sentaurus Device simulation of p+/i/n+ $In_{0.53}Ga_{0.47}As$ diode with T_i=20 nm and N_A=N_D=5 × 10^{18} cm^{-3} on a InP substrate. The models include nonlocal dynamic BTBT, nonlocal intraband tunneling and thermionic emission. The presence of InP reduces the thermal current in forward bias. For the lowest InP doping concentration, the heterojunction tunnel barrier is non-negligible compared to BTBT.

2.4.5 Impact of InP subsrate

All semiconductor stacks discussed in this thesis are MBE grown on InP substrates, and most of the electrical results in the subsequent chapters are extracted through a *back contact* to this substrate. There are significant valence and conduction band offsets at either the InP/$In_{0.53}Ga_{0.47}As$ heterojunction or the InP/$GaAs_{0.5}Sb_{0.5}$ heterojunction, which have a parasitic effect on the BTBT calibration if unaccounted for.

Figure 2.12(a) shows a Sentaurus Device simulation of a p+/i/n+ $In_{0.53}Ga_{0.47}As$ diode with T_i=20 nm on a p-type InP substrate. The InP doping concentration is either 1 × 10^{18} cm^{-3} or 1 × 10^{19} cm^{-3}. The majority carriers that tunnel through the $In_{0.53}Ga_{0.47}As$ bandgap by BTBT, also encounter the heterojunction energy barrier in the valence band. The carriers either tunnel through the barrier by intraband tunneling, or they are thermally excited over the barrier. In the case of InP with N_A=1 × 10^{19} cm^{-3}, the intraband tunneling process is

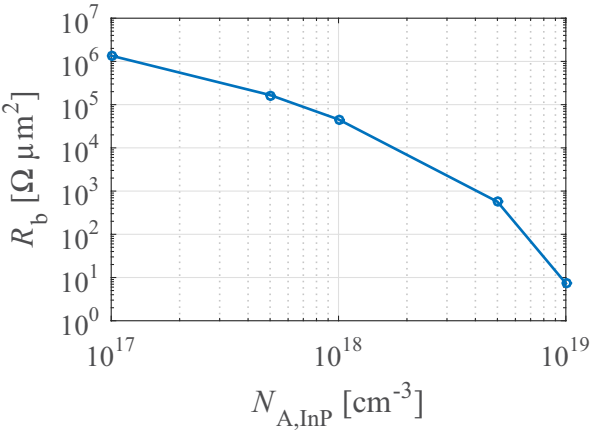


Figure 2.13: Resistance from hole intraband tunneling, extracted from nonlocal mesh intraband tunneling model with the following input parameters. The InP tunneling mass is m_{lh}=0.89 m_0 [48]. The $In_{0.53}Ga_{0.47}As$/InP valence band offset is ΔE_v=0.48 eV [48]. The p+$In_{0.53}Ga_{0.47}As$ dopant concentration is N_A=2 × 10^{19} cm^{-3} and the pInP dopant concentration is variable.

efficient compared to the BTBT process, and the extracted BTBT current is unaffected compared to the case of no InP (figure 2.12(b)). The only difference is a lower thermal current by minority carriers due to the additional energy barrier in the conduction band. For the case of N_A=1 × 10^{18} cm^{-3}, the intraband tunneling process is less efficient compared to the BTBT process. This induces an additional series resistance, causing an unwanted voltage drop over the heterojunction. This resistance is calculated for different InP dopant concentrations using Sentaurus Device, and plotted in figure 2.13.

For the fabrication of $In_{0.53}Ga_{0.47}As$ diodes in the following chapter, only InP substrates with N_A=5 × 10^{17} cm^{-3} were available, so the effect of the heterojunction is not negligible. We will mitigate this effect by increasing the heterojunction area to the full size of the substrate and keeping the $In_{0.53}Ga_{0.47}As$ tunneling junction area small. In section 2.4.6, we calculate how small the tunnel junction needs to be. In section 3.3.3 we will discuss temperature dependent *I-V* measurements which show the thermal excitation over the heterojunction potential barrier is dominant compared to intraband tunneling. The Sentaurus Device commands for the nonlocal tunneling model used for intraband tunneling are listed in appendix A lines 57, 117, 205. The commands for thermionic emission at the heterointerface are shown on line 70.

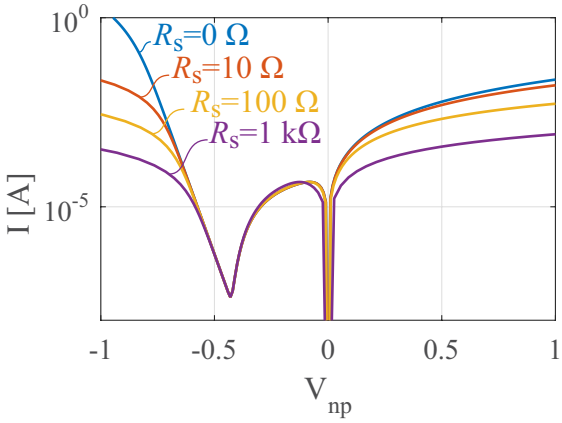


Figure 2.14: Impact of a fixed series resistance in a p+/n+ $In_{0.53}Ga_{0.47}As$ Esaki diode with $N_A{=}N_D{=}2 \times 10^{19}\,cm^{-3}$ with junction area $A_j{=}1\,\mu m^2$. The impact is higher in reverse bias than in forward bias, because in reverse bias there is a higher BTBT current and therefore a higher potential drop over the series resistance.

2.4.6 Design of diode dimensions and contacting schemes

In this section, we identify the different series resistance (R_s) components, and we design the diode dimensions such that this parasitic R_s is negligible compared to the desired 'BTBT resistance' (R_{BTBT}). Figure 2.14 shows the impact of the parasitic R_s on the diode I-V trace. In this simple model, we first consider the 'ideal' $I_{ideal} - V_{ideal}$ trace from the thermal and BTBT current contributions. There is an additional voltage drop over R_s, which stretches the curve along the voltage axis to $I_R - V_R$ using the relations:

$$V_R = V_{ideal} + R_s I_{ideal} \quad \text{and} \quad I_R = I_{ideal} \tag{2.11}$$

We now predict R_s for the specific examples of two contacting schemes in figure 2.15(a) and (b), which are technologically feasible. The first contacting scheme has a *top contact* to n+$In_{0.53}Ga_{0.47}As$ and a *back contact* to the backside of the p-InP substrate. The first important parasitic resistance is $R_{ncontact}$, which is the contact between n+$In_{0.53}Ga_{0.47}As$ and the top contact. The second one is $R_{backcontact}$, which is modeled as a parallel connection of the intraband tunneling resistance at the InP/$In_{0.53}Ga_{0.47}As$ heterojunction directly under the diode, and the spreading resistance component next to the diode. We only

consider intraband tunneling and neglect thermal excitation over the barrier, so this calculation is a worst case scenario.

The second contacting scheme has a *side contact* instead of the *back contact*. It is located at a distance L_{spacing} away from the diode. The current from the diode to the side contact runs either through the thick substrate or through the thin p+$In_{0.53}Ga_{0.47}As$ layer.

For a square $In_{0.53}Ga_{0.47}As$ Esaki diode with T_{i}=10 nm, side length L and other dimensions shown in figure 2.15, the n-contact resistance is given by $R_{\text{ncontact}} = \rho_n/L^2$, where ρ_{n} is the specific contact resistance. The spreading resistances are modeled using the theory of TLM measurements [83], where the total contact resistance including spreading resistance is given by

$$R_{\text{c}} = \frac{\sqrt{\rho_{\text{c}} R_{\text{s}}}}{L} \coth \frac{d}{\lambda} \tag{2.12}$$

where ρ_{c} is the specific contact resistance, R_{s} is the sheet resistance of the semiconductor, d is the length of the contact and λ is the transfer length given by $\lambda = \sqrt{\rho_{\text{c}}/R_{\text{s}}}$.

We use the following material parameters:

- The specific contact resistance at the InP/$In_{0.53}Ga_{0.47}As$ heterointerface is $166 \times 10^3\,\Omega\mu\text{m}^2$. It is taken from figure 2.13 and for InP doping N_{A}=$5 \times 10^{17}\,\text{cm}^{-3}$, which are the only substrates available at the time of fabrication.
- The specific contact resistances of n+$In_{0.53}Ga_{0.47}As$ and p+$In_{0.53}Ga_{0.47}As$ to the metal stack Ti/Au are $R_{\text{c,n}}$=$9.5 \times 10^{-6}\,\Omega\text{cm}^2$ and $R_{\text{c,p}}$=$1.75 \times 10^{-4}\,\Omega\text{cm}^2$. These are measured using TLM measurements.
- The resistivity of n+$In_{0.53}Ga_{0.47}As$ is 0.25 Ωμm and for p+ 252 Ωμm, which we obtain from Hall measurements.

We propose a first set of diode dimensions, where the horizontal dimensions are based on an available photo-lithography mask, and the thicknesses are based on available epitaxially grown stacks. The square diode side length is large: L=200 μm. The thickness of the p+$In_{0.53}Ga_{0.47}As$ layer is t_{ptype}=100 nm. The spacing of the side contact is L_{spacing}=5 μm. All calculated resistances are shown in figure 2.15(c). Compared to R_{BTBT}, R_{ncontact} is negligible. However, R_{back} is much larger than R_{BTBT} over the whole I-V except in the valley region. Similarly, in the case of side contacting, the parallel connection of $R_{\text{side-pInGaAs}}$ and $R_{\text{side-pInP}}$ has higher resistance than R_{BTBT}. The distorted I-V characteristics are calculated with equation 2.11 and shown in figure 2.15(d).

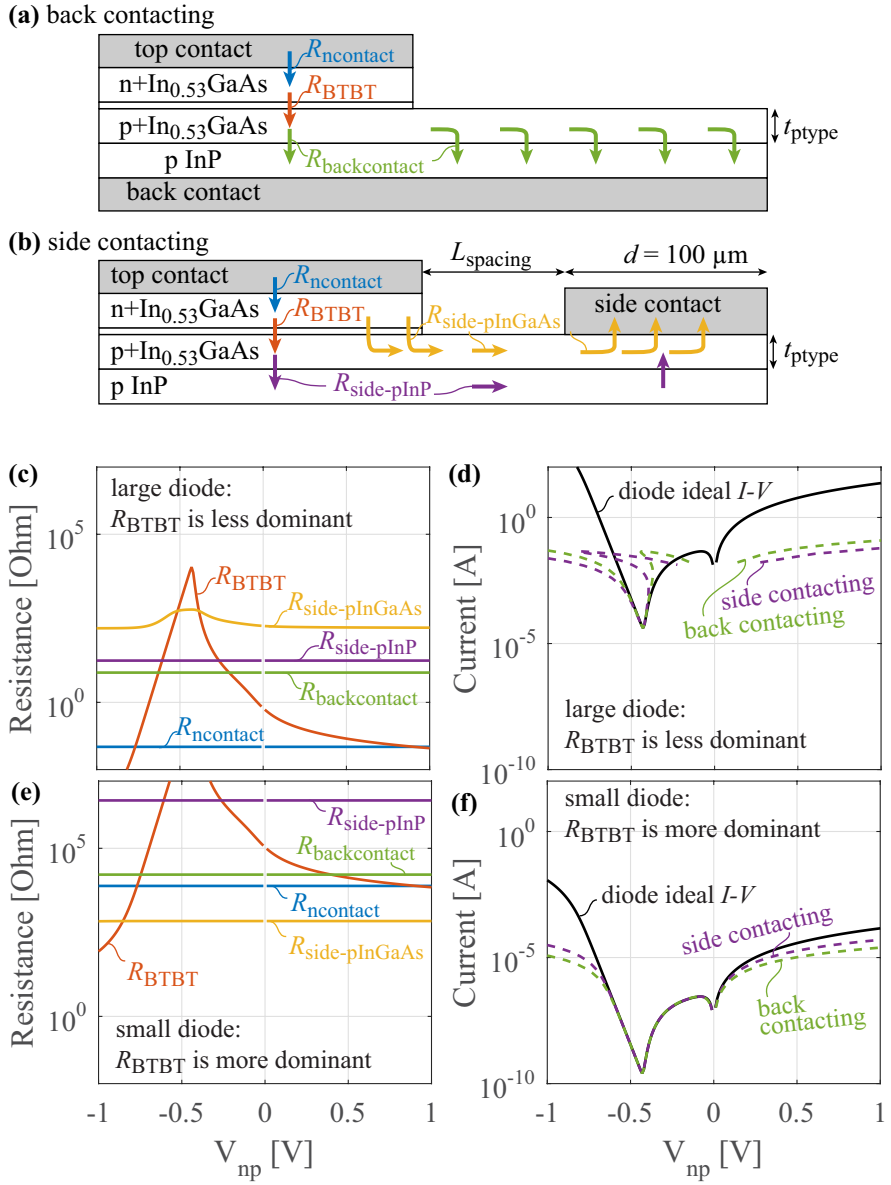


Figure 2.15: The dominant resistance components of a p+/i/n+ $In_{0.53}Ga_{0.47}As$ diode with T_i=10 nm, N_A=N_D=2×10^{19} cm^{-3} on a InP substrate are shown with (a) a back contact to the large InP substrate and (b) a side contact on the thin p+$In_{0.53}Ga_{0.47}As$ layer. (c) The calculated parasitic resistance components in a square diode with 200 μm^2 are dominant compared to R_{BTBT} over nearly the whole voltage range. (d) The ideal *I-V* characteristic is severely stretched for both contacting schemes. (e-f) When the dimensions are optimized, the spreading resistances in the p-$In_{0.53}Ga_{0.47}As$ layer are reduced and R_{BTBT} is measured more accurately.

All voltage values are strongly shifted for both contacting schemes. The NDR peak is still present, but looks like a step function in the case of back contacting, and has a bistable operation point in the case of side contacting. We experimentally confirm this in appendix B.

A second set of dimensions is therefore proposed. The diode side length is reduced to L=0.5 µm. The thickness of the p+$In_{0.53}Ga_{0.47}As$ layer is increased to t_{ptype}=600 nm. $L_{spacing}$ is reduced to 0.1 µm. The results in 2.15(e) show the I-V characteristics are only slightly shifted compared to the ideal case, the NDR region is unaffected by the parasitic resistances and both contacting schemes are viable options. In the case of side contacting, $R_{ncontact}$ is the dominant parasitic resistance. In the case of back contacting, R_{back} is the dominant parasitic resistance. We conclude that larger diodes are more affected by series resistance than smaller diodes, due to the spreading resistance component.

Equation 2.11 is actually a simplified model, since it does not account for the nonuniform electrostatic potential (in the plane of the p-n junction) due to spreading resistance. In the case of a uniform potential over the whole tunnel junction, equation 2.11 is valid and figure 2.14 shows that the peak current value I_p is unaffected by series resistance. Therefore we expect diodes with different diameters and uniform potential to have a constant J_p.

However, if the electrostatic potential at the tunnel junction is nonuniform due to an excessive spreading resistance, the local BTBT current density will also be nonuniform. If we then divide the total BTBT current by the junction area, the apparent J_p will be smaller for larger diodes, due to the stronger impact of spreading resistances. These diodes must then be excluded for BTBT calibration. Therefore, Esaki diodes are more useful compared to Zener diodes, because we can monitor the uniformity of the electrostatic potential using J_p.

During the first year of this thesis, we fabricated $In_{0.53}Ga_{0.47}As$ diodes with the first set of large dimensions using available MBE stacks and a fast fabrication flow. These I-V characteristics, shown in appendix B, are stretched similarly to figure 2.15(d), and have a nonuniform potential at the tunnel junction. Later, we modeled the different series resistance components and we determined the second set of small dimensions. A more complicated fabrication flow was developed in appendix C, which allowed successful BTBT calibration in chapter 3.

2.5 Conclusions

In this chapter, we have introduced the operation of Esaki and Zener diodes, and we have introduced the BTBT models used to predict their characteristics.

There is still uncertainty on the input parameters and the accuracy of these models, therefore we will calibrate them in chapter 3 using experimental Esaki diode measurements. We have made the following conclusions concerning the design of these Esaki diodes:

- We have determined that Esaki diodes with negative differential resistance are more useful than Zener diodes, because the former provide the additional reference points J_{p} and V_{p} to monitor the impact of series resistance, and the uniformity of the electrostatic potential over the tunnel junction.
- We have argued it is better to calibrate BTBT using p+/i/n+ diodes instead of p+/n+ diodes, to mitigate uncertainties of sloped dopant profiles and doping dependent bandgap narrowing.
- We have argued that calibrating BTBT in reverse bias is better than in forward bias, due to the reduced sensitivity to the Fermi level positions.
- We have determined diode dimensions, for which series resistance should be negligible compared to the BTBT resistance over a sufficiently large portion of the I-V profile. We obtained a diode junction area A_{j}=0.5 µm^2, a p+$\mathrm{In_{0.53}Ga_{0.47}As}$ layer thickness t_{ptype}=600 nm, and a side contact spacing L_{spacing}=0.1 µm.

Chapter 3

Calibration of BTBT, SRH and TAT models for InGaAs TFET prediction

The goal of this chapter is to calibrate the Band-To-Band Tunneling (BTBT), Shockley-Read-Hall (SRH) and Trap-Assisted Tunneling (TAT) models using the $In_{0.53}Ga_{0.47}As$ p+/n+ and p+/i/n+ diodes fabricated in appendix C. We then apply these models to predict the performance of $In_{0.53}Ga_{0.47}As$ TFET.

In section 3.1 we start with a literature review of previous BTBT calibration work, and we discuss our own calibration strategy in section 3.2. We proceed with the electrical characterization of the $In_{0.53}Ga_{0.47}As$ p+/n+ and p+/i/n+ diodes in section 3.3. We identify BTBT, SRH and TAT with temperature-dependent current-voltage (I-V) measurements, and we discuss the scaling of the different current components with the junction area. In section 3.4 we determine the dopant profiles by combining Secondary Ion Mass Spectrometry (SIMS) and Capacitance-Voltage (C-V) measurements.

We then calibrate the BTBT model by comparing the measured current densities to simulations. These simulations are performed with either a semi-classical simulator in section 3.5 or a Quantum Mechanical (QM) simulator in section 3.6. In a similar way, we calibrate the SRH and TAT semi-classical models in sections 3.7 and 3.8. Finally, we predict the performance of $In_{0.53}Ga_{0.47}As$ point-TFET and line-TFETs using the calibrated semi-classical simulator in section 3.9.

3.1 BTBT calibration in literature

In 1961, Meyerhofer *et al.* predicted the peak current in Germanium p+/n+ Esaki diodes, and obtain satisfactory agreement with experiments [77]. Meyerhofer used the Kane formalism (introduced in section 2.2.1 on p. 25) with an additional modification term for the density of states. The main approximations were the use of an average electric field at the tunnel junction, and the use of a reduced dopant concentration $N^*=N_\mathrm{A}N_\mathrm{D}/(N_\mathrm{A}+N_\mathrm{d})$ to calculate the electric field. Meyerhofer observed that the BTBT process in Arsenic-doped Germanium diodes do not required a phonon, and can be modeled like direct III-V materials.

In 2012, Pawlik *et al.* from Rochester institute of technology used a similar formalism to predict the peak current in p+/n+ GaAs, $In_{0.53}Ga_{0.47}As$ and InAs Esaki diodes [36, 72]. He used the similar approximations for the density of states, the reduced dopant concentration and average electric field.

Mohata *et al.* from Penn. state university used the same p+/n+ $In_{0.53}Ga_{0.47}As$ Esaki diode measurements from Pawlik, and calibrated the nonlocal mesh BTBT model from Sentaurus Device, introduced in section 2.2.5 [34]. However, box-like dopant profiles were used in the simulations and the series resistance was taken as an additional fitting parameter. Mohata used the calibrated parameters to predict the performance of $In_{0.53}Ga_{0.47}As$ TFET.

Cho *et al.* from Purdue university also used the same p+/n+ $In_{0.53}Ga_{0.47}As$ Esaki diode measurements from Pawlik, and compared these to Quantum Mechanical (QM) simulations including the effect of dopant-dependent bandgap narrowing (DOPBGN) [58]. He concluded DOPBGN causes conduction and valence band offsets at the p+/n+ junction, resulting in an band alignment similar to a staggered gap heterojunction diode.

In 2014, Kao *et al.* from imec presented the calibration of a phonon-assisted nonlocal BTBT model of Sentaurus Device [84] using p+/i/n+ compressively strained SiGe diodes, to predict the performance of SiGe TFET [46]. Kao used dopant profiles obtained by combining SIMS and *C-V* measurements to determine the electrostatic potential in the diodes. Kao's work was performed in parallel with this thesis.

In 2015, Avci *et al.* from Intel presented the calibration of BTBT, SRH and TAT models using Germanium p+/i/n+ diodes, to predict the performance of Germanium TFET [85]. Avci concludes that the density of semiconductor traps is sufficiently low, and does not degrade the Germanium TFET performance.

In this chapter, we aim to go beyond the approximations of reduced dopant

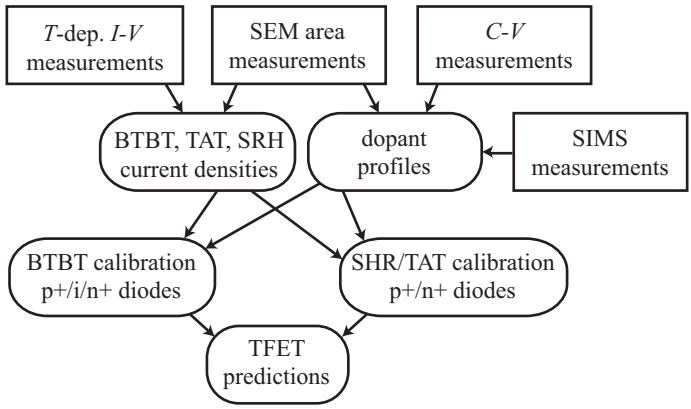


Figure 3.1: Different electrical and physical characterization techniques are combined to obtain accurate BTBT, SRH and TAT calibration and make a prediction of the TFET performance.

concentration, average electric field, and box-like dopant profiles. The models must be applicable to tunnel diodes and TFET with arbitrary dopant profiles. Another goal is to suppress parasitic effects like dopant-dependent bandgap narrowing as much as possible. Therefore we develop our own calibration strategy.

3.2 Calibration Strategy

In this section, we pinpoint four challenges to accurately calibrate the BTBT, SRH and TAT models. The first challenge is the identification of the current mechanisms: BTBT, TAT, SRH, or thermal diffusion current. As introduced in section 2.3, we identify each mechanism with temperature-dependent I-V measurements, and the extracted activation energy. This step is shown in the calibration strategy diagram in figure 3.1. We also measure diodes with different diameters, because these have different area/perimeter ratios. This allows us to verify whether BTBT scales with the diode junction area, and identify whether the TAT and SRH contributions are due to defects in the semiconductor bulk, or defects at the diode perimeter. We are especially interested in the bulk SRH and the bulk TAT contributions, because these are intrinsic properties of the material and its epitaxial growth, and they also apply to a TFET fabricated with a similar epitaxial growth recipe.

The second challenge is the uncertainty on the Jain-Roulston doping-dependent

bandgap narrowing (DOPBGN) model, which we introduced in section 2.2.4. Using parameters from literature [58] and dopant concentrations from SIMS measurements in section 3.4.1, DOPBGN decreases the $In_{0.53}Ga_{0.47}As$ bandgap from 0.74 eV to 0.67 eV in the p+ region and 0.60 eV in the n+ region. This decrease is large, but there is uncertainty on the DOPBGN parameters and its impact on the BTBT rate is still unknown. Also, Sentaurus Device [27] doesn't correctly implement DOPBGN in the region where both dopant types are present. At the transition point between n-type and p-type majority doping, the simulator abruptly switches from the n-type to the p-type DOPBGN parameter set, causing unrealistic conduction and valence band offsets, similar to a heterojunction with staggered band alignment. The QM simulator is not yet capable of including DOPBGN at all. Therefore, we do not calibrate BTBT for the p+/n+ diode, where BTBT occurs in the highly doped regions. Instead we use the p+/i/n+ diodes with intrinsic region thicknesses T_{i}=9, 18, 46 nm, for which BTBT mainly occurs in the (nearly) intrinsic regions.

The third challenge is determining the dopant profiles accurately. BTBT is highly sensitive to the electric field and therefore the local dopant profile. The sensitivity is high in p+/n+ diodes because the dopant concentrations change rapidly in the region where BTBT occurs. The sensitivity is lower in p+/i/n+ diodes because the electric field is nearly constant in the intrinsic region where BTBT occurs. We perform SIMS measurements to obtain the dopant profiles, but there is uncertainty on the concentration, the depth scale, and especially the dopant slopes. Therefore we perform C-V measurements to obtain the junction capacitance, which is related to the depletion region width. Combining SIMS and C-V measurements therefore increases the accuracy of the simulations.

The fourth challenge is the uncertainty on the Fermi level positions, which determine the tunneling energy window and the built-in potential of the diodes. The multivalley model with nonparabolic correction introduced in section 2.2.2 predicts the Fermi level is strongly degenerate and located 0.4 eV above the conduction band edge in the n+ region with N_{D}=2.2 × 10^{19} cm^{-3}. However we have no experimental confirmation for this Fermi level value. In figure 2.5 in the introduction, we observe the BTBT rate is highly sensitive to variations in the Fermi level position of the n-type region when the diode is forward biased, but less when reverse biased. Therefore we calibrate BTBT only in reverse bias.

In summary, we will use the p+/i/n+ diodes with T_{i}=9, 18, 46 nm to calibrate the BTBT rate in reverse bias. However, the p+/n+ diodes will be used to calibrate SRH and TAT in forward bias, because in section 3.3.4 we will determine that bulk SRH and bulk TAT are dominant only for this condition. Furthermore, bulk TAT is dominant only at $T \leq 100$ K, where SRH is partly suppressed.

3.3 Electrical Characterization of InGaAs diodes

All *I-V* characteristics are measured with an *Agilent 4156C* precision parameter analyzer. We verify that all diodes are free of hysteresis, hence charge trapping is negligible. We also verify whether the measurements are impacted by light, because this would cause additional electron-hole pair generation. We perform consecutive measurements with and without the microscope light, and we confirm there is no impact, because all devices are covered with thick $50\times50\mu m^2$ contact pads blocking the incoming light. The only exception to the hysteresis and light sensitivity is one set of cryogenic measurements discussed in section 3.3.3. Note that for all *I-V* plots, we show the absolute value of the current on a logarithmic scale.

In this section we first determine the series resistance to remove its effect. Then, the voltage range of dominant BTBT is extracted with temperature-dependent *I-V* measurements. The scaling of the BTBT current with the area is then analyzed to allow the extraction of the BTBT current density. Additionally, we discuss the Peak to Valley Current Ratio (PVCR).

3.3.1 Impact of series resistance

In section 2.4.6, we predicted that diodes with a larger diameter would have a relatively larger impact of series resistance R_s, due to a spreading resistance component. We experimentally confirm this in figure 3.2(a), which shows the absolute value of the current density as function of reverse bias voltage V_{np} for T_i=18 nm. The current is normalized with the different junction areas A_j as discussed in section 3.3.4. The red dotted line shows characteristics where the impact of R_s has been removed, according to a procedure in the next paragraph. The largest diode with A_j=210 μm^2 (red curve) has stretched out characteristics compared to the smallest diode with A_j=0.15 μm^2 (blue curve). The curve of the largest diode deviates from the exponential trend line at smaller V_{np}, both in forward and in reverse bias, because the largest diode has a higher total current.

We correct the *I-V* characteristics according to the procedure described by Meyerhofer *et al.* [77]. The concept of this method is that we expect the current at high forward bias to increase exponentially, but the V_{np} values have been shifted due to the voltage drop ΔV over R_s. Simulations show an exponentially increasing current with forward bias until high minority carrier injection occurs at $V_{np}<-0.8$ V. To recover this expected exponential dependence, every measured voltage value is 'shifted back' by $\Delta V = I \times R_s$, shown by two arrows in figure 3.2(a). The fitting parameter R_s does not change

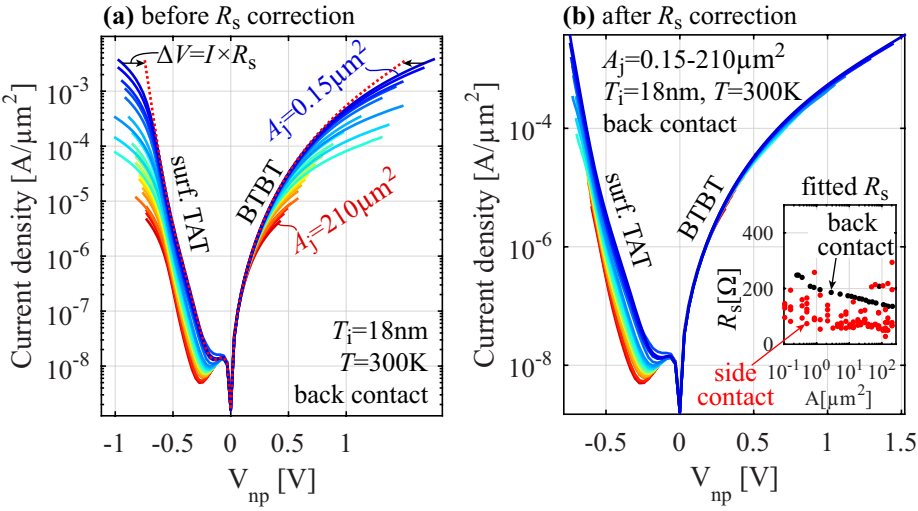


Figure 3.2: (a) The largest diodes are impacted the most by series resistance. (b) After correcting for series resistance, the BTBT current scales with A_j. The current is normalized with the different junction areas, determined in section 3.3.4. The inset shows the fitted R_s, which is lower and more irregular for diodes with side contact than diodes with back contact. Both contact types are shown schematically in figure C.2(j) on p. 180

with V_{np}, but is different for every diode. The resulting I-V characteristics in figure 3.2(b) show that by correcting the exponential current in forward bias, the BTBT current density in reverse bias is constant for all junction areas.

Using this method, we cannot separate the effects of high minority carrier injection and series resistance, which both cause a sub-exponential I-V trace in high forward bias. However, simulations show high injection occurs only for $V_{np}<-0.8\,\mathrm{V}$ for $In_{0.53}Ga_{0.47}As$ with our dopant concentrations. Therefore, the series resistance correction method is reliable only for $V_{np}>-0.8\,\mathrm{V}$.

The inset in figure 3.2(b) shows the fitted values of R_s, one for each diode, which have either a 'back contact' on the back side of the InP substrate (p-type doping $5\times10^{17}\,\mathrm{cm}^{-3}$), or diodes with a Pd/Ti/Pd/Au 'side contact' directly on the p-$In_{0.53}Ga_{0.47}As$. For both types of contacting, R_s decreases only slightly with decreasing A_j. This confirms the dominant spreading resistance component, and validates the motivation to fabricate sub-micrometer size diodes, discussed in section 2.4.6. The resistance for diodes with back contacting is higher, which we attribute to the potential barrier at the p-InP/p-$In_{0.53}Ga_{0.47}As$ heterojunction. The BTBT component is identical with both contacting schemes.

3.3.2 Oscillations due to negative differential resistance

We observe unexpected peaks and plateau regions in the negative differential resistance (NDR) region of some diodes. These peaks are stronger for the larger diodes (shown in figure 3.4(a)), for diodes without intrinsic region and for the staggered gap heterojunction diodes in chapter 4. According to literature, these peaks and plateaus are due to interaction of the negative differential resistance with the measurement circuit, which acts like a inductance/capacitance/resistance (LCR) circuit with a negative resistance component [86]. This causes oscillations in the current, which we confirm with an oscilloscope (not shown).

To prevent these oscillations, Meyerhofer *et al.* recommend stabilizing the diode with a small parallel resistance [77]. We did not perform these measurements, because we are more interested in the reverse bias BTBT current than the NDR region.

3.3.3 Temperature dependent I-V

Temperature dependent *I-V* measurements are the most straightforward way to confirm BTBT in our diodes, and separate it from SRH and TAT. As discussed in section 2.3.1, BTBT in reverse bias usually increases slightly when increasing the temperature, due to temperature-dependent bandgap narrowing (TBGN) and moving Fermi levels. Although this effect cannot be modeled using an Arrhenius law, it corresponds to a low activation energy E_A<0.1 eV. Diffusion or thermal current has a typical activation energy $E_A=E_g$ [87]. For SRH generation/recombination, $E_A=E_g/2$ is typical [87]. For TAT generation/recombination, 0.1 eV<E_A<$E_g/2$ is typical [75, 73, 87].

The measurement results for T_i=0, 9, 18 nm in figure 3.3(a-c) show a small temperature dependence ($E_A \leq 6$ meV) in reverse bias and small forward bias, confirming dominant BTBT. For T_i=9 nm at larger forward bias, the ideality factor of 3 and E_A=0.2 eV suggest dominant TAT [73]. For T_i=18 nm, the ideality factor between 1.5 and 2 at larger forward bias suggests dominant SRH or TAT [73]. For T_i=46 nm (figure 3.3(e-f)), the activation energy at small reverse bias shows dominant BTBT but only at T<350 K. For higher temperatures, E_A=0.69 eV indicating diffusion current. This is because the BTBT generation rate is much lower for this diode due to the lower electric field. The voltage and temperature range of dominant BTBT is thus confirmed for all diodes.

We observe a significant difference between cryogenic *I-V* of T_i=18 nm with side

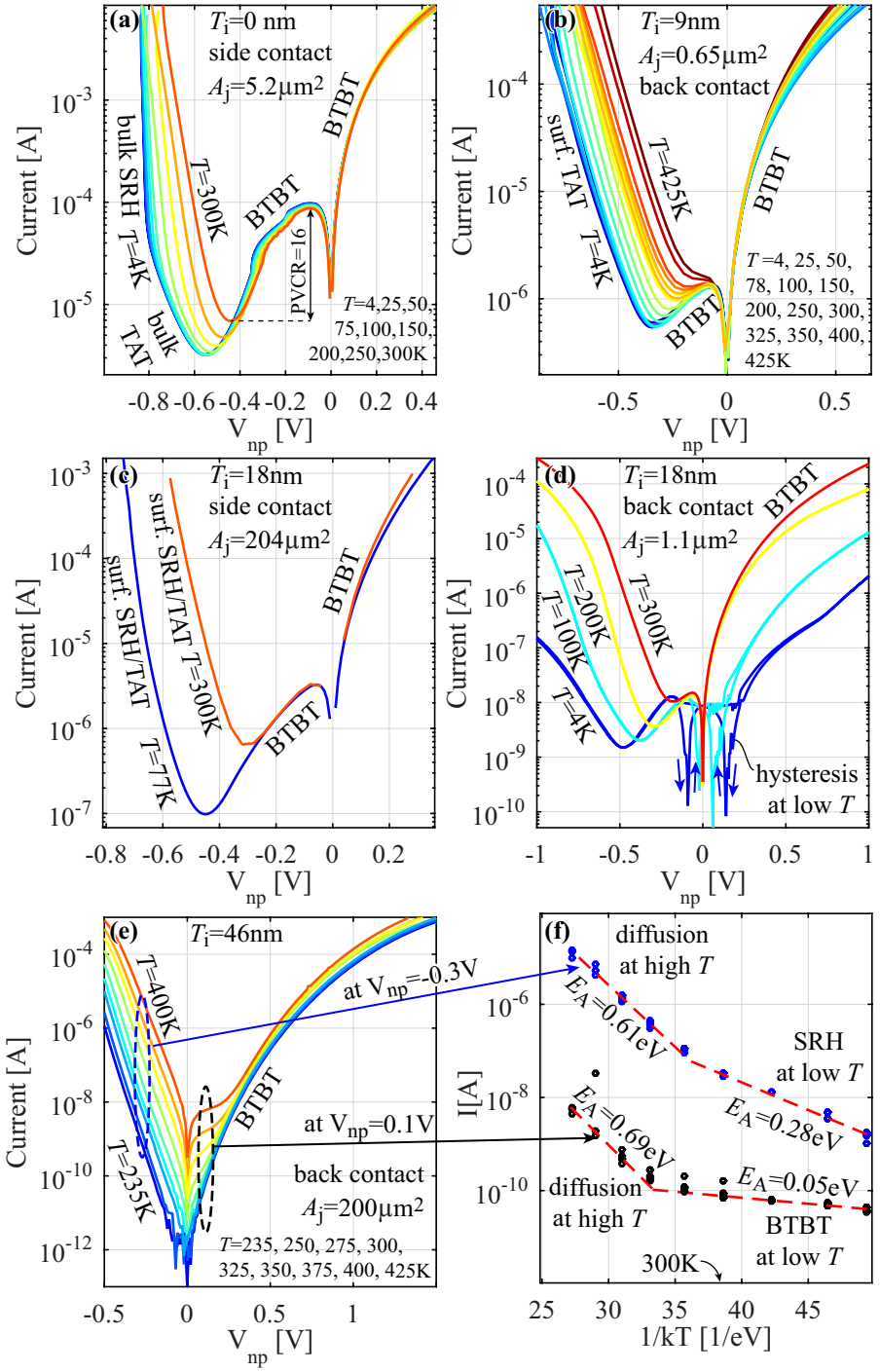


Figure 3.3: T-dep. measurements to identify BTBT, TAT, SRH or diffusion for (a) T_i=0 nm diodes, (b) T_i=9 nm, (c) T_i=18 nm with side contacting, (d) T_i=18 nm with back contacting and (e) T_i=46 nm. (f) shows the activation energy extraction for T_i=46 nm. R_s is corrected as described in section 3.3.1. Bulk and surface components will be identified in section 3.3.4.

contacting and with back contacting (figures 3.3(c) and (d), respectively). The latter shows increasing hysteresis and lower BTBT current when lowering the temperature. When the microscope light is turned on during a measurement, the hysteresis decreases or disappears completely, and the BTBT characteristics are more similar to the diodes with side contacting. At room temperature, the BTBT current of diodes with side contacting and back contacting is the same.

We strongly suspect this unusual behavior is due to the heterojunction between the p-InP substrate and the p-$In_{0.53}Ga_{0.47}As$. In case of diodes with back contacting, electron hole pairs are generated at the $In_{0.53}Ga_{0.47}As$ tunneling junction. Holes flow to the back contact by drift/diffusion, but encounter the large potential barrier at the p-$In_{0.53}Ga_{0.47}As$/p-InP heterojunction, shown in figure 2.12(a). This blocks the current flow, causes a charge pile-up in the p-$In_{0.53}Ga_{0.47}As$ region, which shifts the electrostatic potential and lowers BTBT. When the microscope light is turned on, or when the temperature is increased, the holes gain sufficient energy to overcome the potential barrier at the heterojunction and the full BTBT current is restored. In case of side contacting, the holes do not have to cross the p-$In_{0.53}Ga_{0.47}As$/p-InP heterojunction and this behavior is not observed. For the upcoming calibration, we only use data from samples with side contacting, or samples with back contacting at room temperature or higher where this effect is negligible.

3.3.4 Junction Area extraction and area scaling

In this section, we determine whether the BTBT, SRH and TAT current originates from the diode perimeter (BCB/$In_{0.53}Ga_{0.47}As$ interface) or the diode bulk (inside the $In_{0.53}Ga_{0.47}As$), by considering diodes with different junction areas A_j. The areas are mainly determined by the 'MESA' e-beam lithography step on the SiO_2 hard mask, but they are slightly smaller due to a sloped SiO_2 dry etching and undercutting during the $In_{0.53}Ga_{0.47}As$ wet etching. Therefore, due to slight variations in the wet etching speed and time, not all samples are etched equally, which causes small variations D_{var} of the diode diameter.

In section C.8 on p. 195, we used SEM to measure a set of diode junction areas on a 'reference' sample. We call these $A_{j,SEM}$. We then apply these dimensions to other 'device' samples, and verify whether BTBT current scales with $A_{j,SEM}$. For the largest diode dimensions we obtain area scaling, but for the smallest dimensions the current is lower than expected (plot not shown). This is not caused by defects at the perimeter, because these would cause a higher than expected current. We attribute this to slightly overetching a 'device' sample compared to the 'reference' sample. This reduces all diode diameters by D_{var}.

We fit the parameter D_{var} using electrical measurements, by assuming that BTBT scales with A_{j}. The relation between A_{j} and D_{var} is given by:

$$A_{\mathrm{j}} = \left(\sqrt{A_{\mathrm{j,SEM}}} - D_{\mathrm{var}}\right)^2 \quad \text{for square and diamond shaped diodes} \tag{3.1}$$

$$A_{\mathrm{j}} = \pi \left(\sqrt{\frac{A_{\mathrm{j,SEM}}}{\pi}} - \frac{D_{\mathrm{var}}}{2}\right)^2 \quad \text{for round shaped diodes} \tag{3.2}$$

We obtain the following realistic values for the different samples:

- D_{var}=100 nm for T_{i}=0 nm with side contact
- D_{var}=70 nm for T_{i}=9 nm with back contact
- D_{var}=200 nm for T_{i}=18 nm with side contact
- D_{var}=150 nm for T_{i}=18 nm with back contact.

In the log-log plot in figure 3.4(b), we map the peak current of diodes with T_{i}=9 and 18 nm (at V_{np}=−70 mV, near the BTBT peak current), versus the determined A_{j}. We obtain $I \sim {A_{\mathrm{j}}}^n$, with the slope of the linear fit n=1.0. Therefore, we are confident the over-etching model is correct, and BTBT scales with the diode area.

For T_{i}=46 nm, fabrication issues occurred and only the largest diodes with A_{j}=200 µm^2 could be measured. However, we are confident bulk BTBT is dominant in reverse bias, because the activation energy is low (E_{A}=0.05 eV, figure 3.3(f)), and T_{i}=0, 9, 18 nm also have dominant bulk BTBT in reverse bias.

When T_{i}=0 nm is forward biased in the SRH and TAT regime, the current also scales with the area (figure 3.4(a)). We will therefore use this data for the calibration of bulk SRH and TAT models in sections 3.7 and 3.8. When T_{i}=9 and 18 nm are forward biased in the TAT/SRH regime (V_{np}=−0.5 V), we obtain a scaling exponent n=0.5, (figure 3.4(c-d)). The current scales with the square root of the area, which is proportional to the perimeter. This TAT/SRH current therefore originates at the rough and defect-rich diode perimeter.

3.3.5 Peak-to-Valley Current Ratio

The Peak-to-Valley Current Ratio (PVCR) is a convenient figure of merit for tunnel diodes. The peak current captures the BTBT rate, which should be high

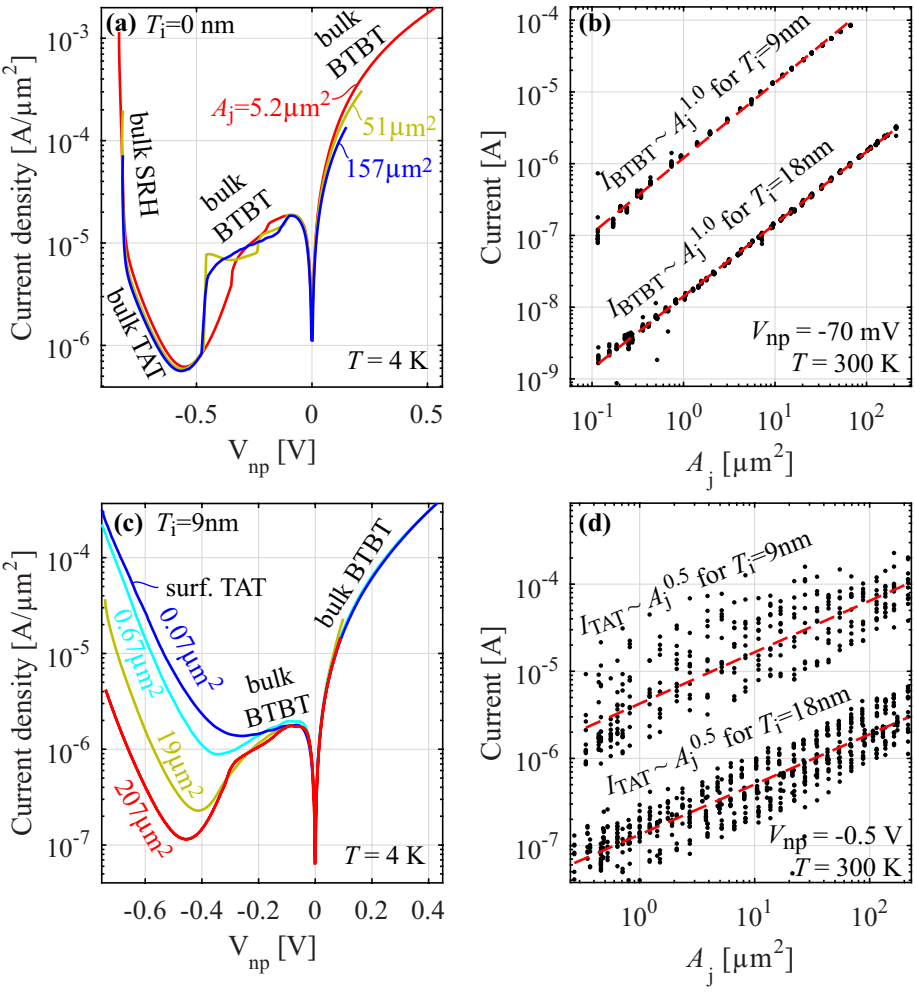


Figure 3.4: We perform measurements on diodes with different junction areas A_j to identify area or perimeter scaling. (a) For T_i=0 nm, SRH, TAT and BTBT scale with the junction area. Therefore the current originates in the bulk of the device. (c) For T_i=9 nm, BTBT scales with the junction area but TAT/SRH in forward bias scales with the perimeter. (b,d) For T_i=9, 18 nm, the BTBT current is proportional to the junction area, but the SRH/TAT current is proportional to the square root of the area, the diode perimeter. These results are obtained by assuming that overetching the diodes causes a reduction in diode diameters D_{var}, which is different for every sample.

in a TFET, and the valley current captures TAT/SRH current, which should be low in a TFET. It is therefore a benchmark of the epitaxial quality of the material. However, the PVCR is not useful when perimeter defects determine the valley current, which is the case for most of our devices.

For diodes with T_i=9 and 18 nm, smaller diodes have a relatively larger amount of perimeter SRH/TAT, and therefore the PVCR is lower (example in figure 3.4(c)). For the largest available devices with T_i=9, 18 nm, the room temperature PVCR is 6 for square diodes and 3 for round diodes. We attribute this to the anisotropic wet etching. In the previous chapter, the SEM images in figure C.8(e-h) showed rougher and possibly more defective sidewalls for the round shaped diodes compared to square and diamond shaped diodes. For T_i=46 nm at room temperature and forward bias, the BTBT current is lower than the SRH and diffusion current and we do not observe NDR. For T_i=0 nm at room temperature, the SRH valley current originates from the bulk of the diodes, and we obtain PVCR=16 (figure 3.3(a)), which is a record for $In_{0.53}Ga_{0.47}As$ homojunctions [36, 41].

3.4 Extraction of the diode dopant profiles

Before we run simulations to calibrate the BTBT, TAT and SRH models, we determine the dopant profiles with realistic error bars for T_i=0, 9, 18, 46 nm. We perform complementary SIMS and C-V measurements to achieve a higher accuracy.

3.4.1 Dopant profiles for Ti=18, 46nm

The dopant concentration of T_i=18, 46 nm is determined with SIMS. The primary beam is a 250 eV Oxygen beam and the mass separation is performed by a magnetic sector. Both dopant types are measured at the same time, and each SIMS measurement is performed twice to confirm tool stability. Figure 3.5(a-b) shows the Silicon concentration is N_{Si}=2.2×10^{19} cm^{-3} (n-type dopants) and the Beryllium concentration is N_{Be}=1.7×10^{19} cm^{-3} (p-type dopants) in the respective neutral regions. Concerning the Silicon background concentration, the SIMS detection limit is $N_{Si,min}$=2×10^{17} cm^{-3}. However, measurements on previous samples from this MBE tool have resulted in values about 1×10^{16} cm^{-3} so we consider this value more realistic. The Beryllium background concentration in the so-called intrinsic region is 2×10^{17} cm^{-3}.

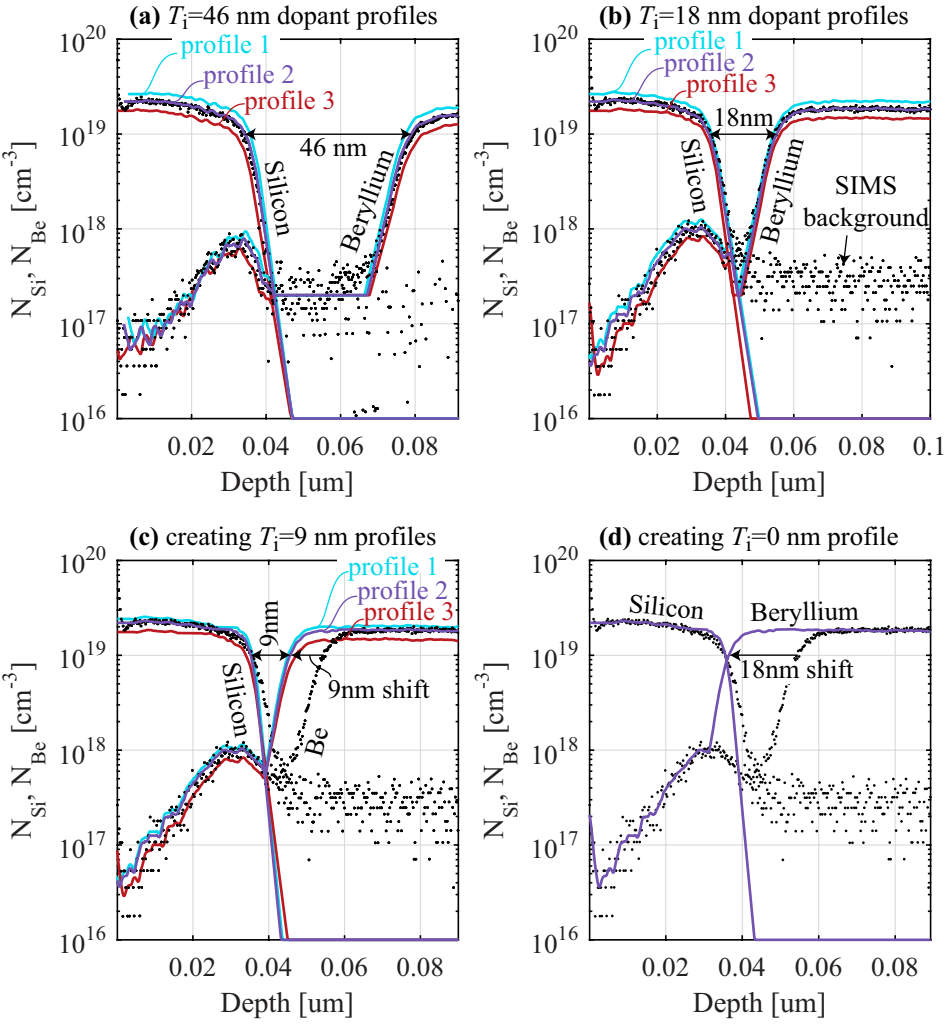


Figure 3.5: The SIMS dopant profiles for (a) T_i=18 nm and (b) T_i=46 nm are shown by the black dots. For each diode we generate three possible dopant profiles (full lines) within the SIMS error bars, using complementary C-V measurements and simulations. For (c) T_i=9 nm, no SIMS measurement was performed, and the possible dopant profiles are obtained by shifting the SIMS Beryllium profile of T_i=18 nm by 9 nm and obtaining a C-V match. (d) No SIMS or C-V are available for T_i=0 nm, so we shift the Beryllium profile 2 of T_i=9 nm by an additional 9 nm to obtain the full line.

In the intrinsic region, the dopant concentrations decrease exponentially with depth. We define the intrinsic region thickness T_{i} as the distance between the two points where the concentration has decreased to 50% of its original value. Figure 3.5(a-b) shows T_{i} matches exactly with the designed values of the MBE growth, for both T_{i}=18, 46 nm. Since the n- and p-type dopant concentrations are not excessively high, activation is assumed 100%. Furthermore, simulations have shown that even if the activation in the neutral regions is 70%, the change in electric field at the tunnel junction is negligible.

3.4.2 Dopant profile for Ti=0, 9nm

No SIMS measurement was performed for T_{i}=0 and 9 nm. We create new dopant profiles for these diodes based on the knowledge that for both T_{i}=18, 46 nm, the target T_{i} matches the measured T_{i}. We extrapolate the SIMS data for T_{i}=18 nm by shifting the Beryllium profile by 18 and 9 nm towards the Silicon-doped region (figure 3.5(c-d)). The Beryllium peak in the n-type region is kept identical.

3.4.3 Sources of uncertainty on the dopant profiles

Uncertainties on the width of the intrinsic region and the dopants at the edge of the intrinsic region have the largest impact on the electric field, and must be taken into account. Only a small degradation of dopant downslopes during the SIMS measurement is possible, given the low surface roughness of the samples (RMS=0.2 nm, as measured by AFM). There is also some uncertainty on the depth scale (±5%) and the absolute concentration of dopants measured (±20%).

3.4.4 C-V measurements

Due to the uncertainties mentioned above, C-V measurements are used as a complementary technique to determine the junction capacitance, which is linked with the depletion region width. These measurements are carried out on the same devices for which the BTBT current density is extracted, and thus provide information on the local dopant profile. We will then compare these C-V measurements to Sentaurus Device AC simulations with imported SIMS dopant profiles.

The impedance of the diodes is measured with a *Agilent 4284A precision LRC meter*. A parallel capacitance - parallel conductance $C_{\mathrm{p}} - G_{\mathrm{p}}$ equivalent circuit is used to reflect the high conductive component. The complex admittance $Y = G_{\mathrm{p}} + j\omega C_{\mathrm{p}}$ is then measured. C_{p} can only be extracted accurately if ωC_{p}

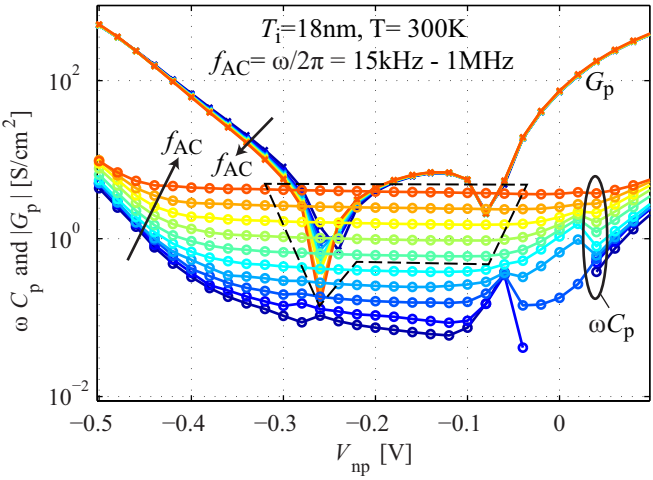


Figure 3.6: The susceptance ωC_p and conductance G_p of T_i=18 nm are shown at different frequencies f=15 kHz to 1 MHz. The direction of the arrows indicate higher frequencies. C_p can be extracted if ωC_p is larger than or comparable to G_p. These conditions are met in the valley region V_{np}=-0.1 to -0.3 V and at sufficiently high frequencies (f=100-630 kHz), indicated by the dashed region.

is similar or higher than G_p. To increase ωC_p, the frequency range $f = \omega/2\pi$ is taken sufficiently high; 100 kHz - 630 kHz for T_i=18, 46 nm, and 400 kHz - 640 kHz for T_i=9 nm. To decrease the conductive leakage G_p, the diodes are biased in the valley region where BTBT and other recombination currents are low. The range where C_p can be extracted is shown by the dashed line in figure 3.6 for T_i=18 nm. For T_i=9 nm, G_p is too high at room temperature, and the C-V measurements are done at T=77 K to decrease conductance by TAT recombination. Under these conditions, C_p is frequency independent and increases slightly with forward bias because the depletion region becomes more narrow. We could not obtain the capacitance for T_i=0 nm due to excessive conductance.

All C-V characteristics are measured on the largest diodes with A_j=216 µm^2 to have the highest capacitance signal. For easier probing, most C-V measurements are done on devices encapsulated in BCB, with a 2900 µm^2 contact pad on top of the device and surrounding BCB. Therefore, the measured capacitance is a parallel circuit of the junction capacitance and a parasitic pad capacitance. The correct for the latter, we perform C-V measurements on contact pads where no diodes are present. This pad capacitance is measured separately on every sample, since it depends on the thickness of the underlying BCB. The pad capacitance

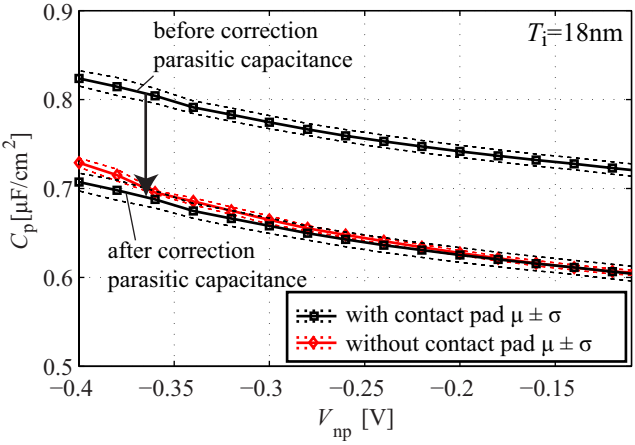


Figure 3.7: The capacitance of devices with and without contact pad match when the measured capacitance is corrected by subtracting the parasitic contact pad capacitance. The average μ (full lines) and standard deviation σ (dotted lines) are taken over 6 devices.

varies between 2.5×10^{-13} F and 3.1×10^{-13} F. The junction capacitance of the diodes is then determined by subtracting the pad capacitance from the total measured capacitance. In order to validate this approach, the junction capacitance for T_i=18nm was extracted from devices with and without contact pad. After the correction for the parasitic pad capacitance, the capacitances of both device types match, as shown in figure 3.7.

Figure 3.8 shows the measured junction capacitance for T_i=9, 18, 46 nm. The C-V measurements have a systematic uncertainty ν and a statistical uncertainty σ. Measured over 10 devices, the standard deviation on the capacitance is about 1% of its average value. Possible systematic errors on the extraction of the diode area with SEM are ±2% uncertainty on the SEM calibration, ±0.5% uncertainty due to the resolution of the images, ±0.2% uncertainty on the estimation of the junction location. The possible systematic error of the capacitance measurement is[88] ±1.5%, given the 2 m cable length, C=1×10^{-12} F and f=600 kHz.

3.4.5 Combining C-V and SIMS measurements

Using Sentaurus Device AC simulations, three dopant profile sets (profiles 1, 2, 3 in figure 3.5(a-c)) are generated to match the experimentally measured capacitance. Profile sets 1, 2, 3 are based on the SIMS profiles and lie within

the range of SIMS uncertainties. As shown in figure 3.8, profiles 1 match the highest possible capacitance values, and would give the highest possible BTBT current. Profiles 2 match the capacitance values in the case of zero systematic and statistical error. Profiles 3 match the lowest possible capacitance values, and would give the lowest possible BTBT current. The simulated and measured capacitance values match over the full voltage range where they can be extracted.

The possible dopant profiles 1,2,3 for T_{i}=18 nm are obtained by scaling the dopant concentration by 1.2, 1, 0.8, scaling the depth values by 1.05, 1.05, 1, and reducing the dopant downslopes to 90%, 90%, 80% of their original value, respectively. For T_{i}=46 nm, the concentration is scaled by 1.2, 1, 0.8, the depth by 0.95, 0.97, 1.02, and the dopant downslopes are kept identical. For T_{i}=9 nm, the concentration is scaled by 1.1, 1, 0.8, the depth by 1.05, 1.05, 1.02, and the downslopes to 50%, 50%, 65% of their original value, respectively.

A remarkable conclusion of these simulations is different dopant profiles which result in a similar simulated capacitance, also give a very similar simulated BTBT current. This is due to the strong correlation between the junction capacitance and the BTBT current. The capacitance is given by the depletion width and the fluctuating carrier density at both sides of the depletion region. Similarly, the BTBT density is given by the tunneling length and the carrier density at both sides. In other words, the BTBT calibration is not very sensitive to which types of adjustments are made to the dopant profiles, as long as the capacitance simulated with these profiles matches the measured capacitance. Therefore it is crucial to achieve a match between the simulated and the measured C-V for a high-accuracy BTBT calibration.

Since we cannot obtain the capacitance of T_{i}=0 nm, we shift profile 2 of T_{i}=9 nm by an additional 9 nm to obtain the full line in figure 3.5(d). This is less accurate than obtaining a full C-V match, but this dopant profile will be used for SRH and TAT calibration only.

3.5 Calibration of semi-classical BTBT model

In this section, we calibrate the BTBT parameters using the previously discussed dopant profiles and the measured BTBT current density. Then we discuss the error bars of the calibration and we compare the results to the theoretical prediction.

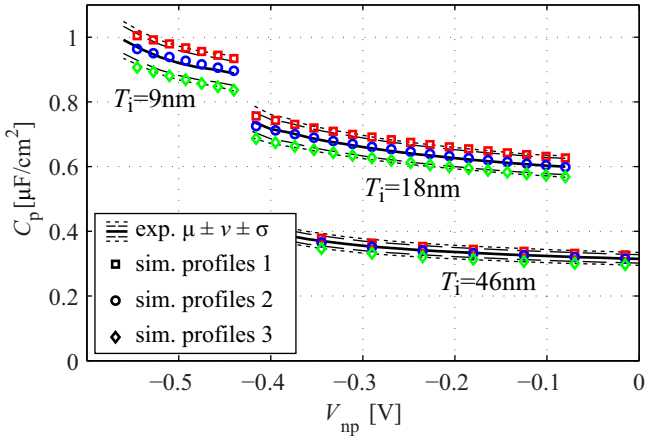


Figure 3.8: The average measured capacitance (μ, full lines), the additional systematic error ($\mu\pm\nu$, broken lines) and additional standard deviation ($\mu\pm\nu\pm\sigma$, dashed lines) are shown for T_i=9, 18, 46 nm. Simulations of C-V using profiles 1, 2, 3 reflect the uncertainty on the measured C-V. T_i=9 nm are measured using contact pads at T=77 K. T_i=18 nm are measured both with and without pads at T=300 K (figure 3.7). For T_i=46 nm, the junction capacitance is comparable to the parasitic pad capacitance, and only devices without contact pads are considered (T=300 K).

3.5.1 Band structure models and parameters.

We use the temperature and dopant dependent bandgap narrowing models discussed in sections 2.3.1-2.2.4. The carrier density and Fermi level positions are calculated using Fermi Dirac statistics and the multivalley band structure with nonparabolic correction introduced in section 2.2.2. Using these models, the electron quasi Fermi level in n-type $In_{0.53}Ga_{0.47}As$ neutral region with N_{Si}=$2.2\times10^{19}\,cm^{-3}$ is 0.40 eV above the conduction band edge. The hole quasi Fermi level in the p-type $In_{0.53}Ga_{0.47}As$ neutral region with N_{Be}=$1.7\times10^{19}\,cm^{-3}$ is 0.04 eV below the valence band edge.

3.5.2 Calibration of the BTBT parameters

In Sentaurus Device, BTBT is implemented with the dynamic nonlocal BTBT model discussed in section 2.2.5 on p. 31. Two fully equivalent sets of input parameters can be provided: The first set is A_{BTBT}, B_{BTBT}, and the ratio m_v/m_c. This ratio determines the asymmetric Franz dispersion relation

	lower limit	recommended	upper limit	theory
A_{BTBT} [$\mathrm{cm^{-3}s^{-1}}$]	1.1×10^{20}	1.3×10^{20}	1.6×10^{20}	1.6×10^{20}
B_{BTBT} [$\mathrm{Vcm^{-1}}$]	6.0×10^{6}	5.7×10^{6}	5.4×10^{6}	5.6×10^{6}
$m_{\mathrm{v}}/m_{\mathrm{c}}$	1.21	1.21	1.21	1.21
m_{c} [m_0]	0.050	0.045	0.041	0.043
m_{v} [m_0]	0.061	0.055	0.049	0.052
g	1.3	1.6	2.1	2.0

Table 3.1: The lower limit, recommended values and upper limit for the calibrated BTBT parameters are determined with dopant profile set 1, 2 and 3, respectively. The BTBT model requires either the parameters in the top three rows, or the equivalent parameters in the last three rows. The Franz dispersion relation (p. 31) is calculated with the ratio $m_{\mathrm{v}}/m_{\mathrm{c}}$, which we take from literature. The values in the last column are from the Keldysh and Kane theory, and are within the calibrated range.

(introduced in figure 2.8 on p. 2.8), and is taken from literature [48]. Alternatively, we could provide the input parameters m_{c} and m_{v} directly, in addition to the degeneracy g. We choose to calibrate the first set of parameters, and subsequently calculate the second set. We only consider the BTBT current in reverse bias, because the BTBT rate is significantly less sensitive to the position of the Fermi levels than in forward bias, as shown in figure 2.5 on p. 30.

First, the dopant profile set 1 (for T_{i}=9, 18, 46 nm) is imported in the simulator. The parameters A_{BTBT} and B_{BTBT} are then modified until a good fit of the BTBT current is obtained for the three diode types at the same time. The results are shown in figure 3.9, and determine the lower boundary for the parameters. This process is then repeated for profiles 2 and 3. The resulting calibrated BTBT parameters are shown in table 3.1. Figure 3.9 shows we achieve an excellent agreement between the measured and simulated current density, with a maximum difference of 20%.

The uncertainty on the BTBT generation rate is determined by the difference between the upper limit and lower limit in table 3.1, but also depends on the electric field F at the junction. Equation (2.1) on p. 25 shows that G_{BTBT} depends exponentially on B_{BTBT} when $F \ll B_{\mathrm{BTBT}}$, but scales linearly with A_{BTBT} when $F \gg B_{\mathrm{BTBT}}$. For TFETs in the on-state, where the source junction electric field is typically F=4 MV/cm, the uncertainty on the generation rate is only ±30%. For MOSFET in the off-state, where the drain junction electric field

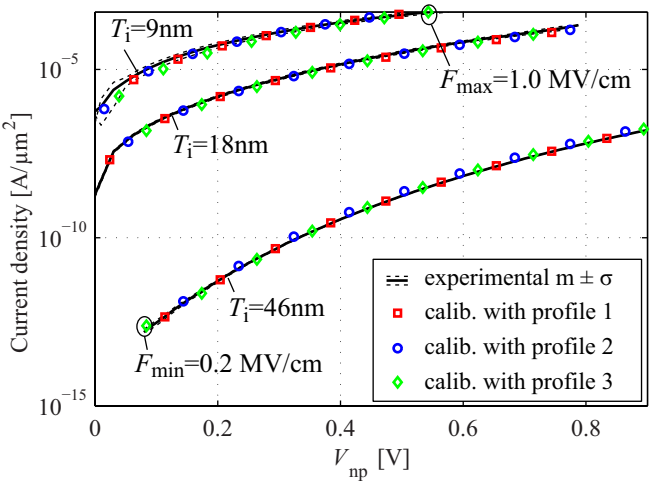


Figure 3.9: With the calibrated parameters A_{BTBT} and B_{BTBT} shown in table 3.1, the simulated and experimental BTBT current match over the full range of electric fields (F=0.2-1 MV/cm). The dotted lines indicate the standard deviation of 64, 32, 9 devices for T_{i}=9, 18, 46 nm, respectively.

is typically F=1 MV/cm [89], the uncertainty on BTBT generation is ±50%.

We now compare the calibrated parameters to their theoretically predicted values. According to the formalism by Keldysh and Kane [47] and the correction by Vandenberghe *et al.* [67],

$$A_{\mathrm{BTBT}} = \frac{\mathrm{g} m_{\mathrm{r}}^{1/2} (qE_0)^2}{\pi h^2 \sqrt{E_{\mathrm{g}}}} \tag{3.3}$$

$$B_{\mathrm{BTBT}} = \frac{\pi^2 m_{\mathrm{r}}^{1/2} E_{\mathrm{g}}^{3/2}}{qh} \tag{3.4}$$

where g is the degeneracy factor, q is the elementary charge and h is Planck's constant. The reduced tunnel mass m_{r} is given by $(m_{\mathrm{e}}^{-1} + m_{\mathrm{lh}}^{-1})^{-1}$. Using the electron effective mass $m_{\mathrm{e}} = 0.043\, m_0$[64] and hole effective mass $m_{\mathrm{lh}} = 0.052\, m_0$[90], we obtain $A_{\mathrm{BTBT}} = 1.6{\times}10^{20}\,\mathrm{cm^{-3}s^{-1}}$, $B_{\mathrm{BTBT}} = 5.6{\times}10^{6}\,\mathrm{Vcm^{-1}}$, which are within the range of calibrated values (table 3.1).

3.6 Quantum mechanical BTBT calibration

In this section, the input parameter of a QM simulator is calibrated using the values obtained in table 3.1, and compared to the theoretically predicted value. Finally, the diode I-V characteristics of the QM simulator and semi-classical simulator are compared.

The QM simulator is developed by Devin Verreck from imec and introduced in section 2.2.6 on p. 35. It is based on the envelope function formalism, while applying quantum transmitting boundary conditions [63] at the contacts. This implementation only considers two bands, so there is only coupling between these bands in the transport direction, and an effective mass approximation is applied in the orthogonal direction. The only input parameters for this simulator are the $\mathbf{k}\cdot\mathbf{p}$ interband momentum matrix element $\mathbf{P}$ between conduction and valence band, the bandgap, and the effective mass for the orthogonal direction. $\mathbf{P}$ is a measure for the coupling strength between the respective bands and is usually listed in units of energy as E_P [64]:

$$E_\mathrm{P} = \frac{8\pi^2 m_0}{h^2}\mathbf{P}^2. \tag{3.5}$$

We calibrate E_P from B_BTBT with the relation

$$B_\mathrm{BTBT} = \frac{\pi^2 E_g^2 m_0}{2h\sqrt{E_\mathrm{p} m_0/2}} \tag{3.6}$$

derived from calculations by Kane [47]. Using the values from table 3.1, the range of calibrated values $E_\mathrm{P} = 13.5,\ 15,\ 16.5\,\mathrm{eV}$ is obtained, with respectively the lower limit, recommended value, and upper limit.

From theory, we can calculate the expected value of E_P in a 2-band description with no perturbation from other bands or spin-orbit interaction from [64]:

$$\frac{m_0}{m_e} = 1 + \frac{E_\mathrm{P}}{E_\mathrm{g}}. \tag{3.7}$$

We then obtain the theoretical prediction E_P=16.5 eV, which is within the range of calibrated E_P.

It should be noted that E_P differs from that in reference [64], where a value of 25.3 eV is recommended. This larger value is a result of the higher band perturbations included in the 8-band model, which necessitate an increase in E_P to retain the same effective mass (compare equation (2.15) in reference [64] to equation (3.7)). E_P obtained in this work is therefore valid for models which do not perturbatively include the effects of higher bands.

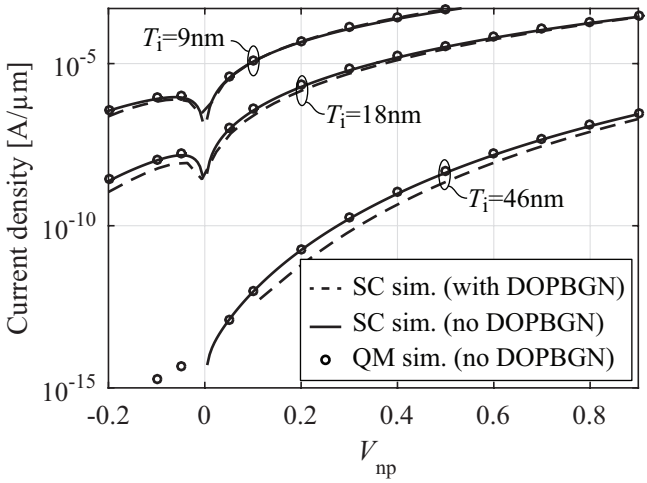


Figure 3.10: The BTBT current calculated by the QM simulator (without DOPBGN) and semi-classical (SC) simulator (without DOPBGN) are in good agreement. The former uses $E_P = 15\,\text{eV}$ and a electron/light hole effective mass approximation in the transverse direction. The latter uses the recommended parameters in table 3.1. The potential is calculated with dopant profile set 2. The SC simulations (with DOPBGN) from figure 3.9 are included for comparison.

In order to validate this calibration method using equation (3.6), the diode electrostatic potential profile is calculated by the semi-classical simulator. DOPBGN is deactivated since this is not supported by the QM simulator. The electrostatic potential is then imported in the QM simulator, and the BTBT current calculated by both simulators is compared. Figure 3.10 indeed shows a very good agreement between both I-V curves. This agreement is expected, as the minimum diameter of the working diodes is about 200 nm, which is large enough not to observe quantum confinement effects.

The 2-band k·p QM simulations in figure 3.10 are performed with the effective mass approximation in the transverse direction, considering the electron and light hole effective masses. However, subsequent comparison with 15-band k·p QM simulations show the heavy hole effective mass should be used in the transverse direction. Therefore, using the parameter $E_P = 15\,\text{eV}$ in 15-band k·p QM simulations overestimates the BTBT current by a factor 1.6 compared to the calibration. This difference is also shown in figure 2.7 on p. 33.

3.7 Calibration of SRH model

We have given a brief introduction on the SRH generation/recombination mechanism in section 2.3.5 on p. 41. We will now identify which regions of the I-V curves have dominant SRH from temperature-dependent I-V, and separate SRH by perimeter defects and bulk defects using diodes of different dimensions. Then we calibrate the bulk SRH contribution. In section 3.9 we will apply the SRH model to TFET simulations.

3.7.1 Analysis of electrical results

Figure 3.3(a) on p. 60 shows the temperature dependent I-V curves of T_{i}=0 nm (the p+/n+ diode). In forward bias, the current increases exponentially with forward bias with an ideality factor of 1.2 between 100 K$\leq T\leq$300 K. This means the current-voltage dependence has an inverse slope of $\approx 1.2\times\ln(10)kT/q$, which corresponds to 74 mV/dec at room temperature. This indicates recombination by the SRH process.

Alternatively, the current could be associated with Auger recombination, where an electron is injected in the p+ region, it recombines with a hole and the energy is released to a third particle (electron or hole). A similar process occurs in the n+ region. However, the Auger process is associated with an ideality factor of 1, which is not observed in our case. We will further verify the possibility of Auger recombination with simulations in section 3.7.4.

Figure 3.4(a) on p. 63 shows the SRH recombination current scales with the junction area, meaning we can use this data to calibrate the SRH model, and simulate SRH generation in a TFET.

For T_{i}=46 nm, the activation energy plot in figure 3.3(f) on p. 60 shows dominant BTBT at V_{np}=0.1 V and dominant SRH at V_{np}=−0.3 V at room temperature, with an ideality factor of 1.05 for 300 K$\leq T\leq$425 K. However, only the largest diodes could be measured due to fabrication issues, and therefore we are unable to verify whether this current in forward bias scales with the junction area, or with the surface. For T_{i}=9 nm in figure 3.4(c-d) on p. 63, and T_{i}=18 nm, we confirm that the exponentially increasing current in forward bias scales mainly with the diode perimeter. This means surface SRH or surface TAT is dominant over bulk SRH. Therefore, we will calibrate the SRH model by using only T_{i}=0 nm. For all other diodes, we impose the condition that the simulated SRH current must be lower than the measured current.

3.7.2 Dopant-dependent SRH model and assumptions

In Sentaurus device [27], the SRH recombination rate is given by

$$R_{\mathrm{SRH}} = \frac{np - F_{\mathrm{n}}F_{\mathrm{p}}n_i^2}{\tau_{\mathrm{p}}(n + F_{\mathrm{n}}n_{\mathrm{i}}) + \tau_{\mathrm{n}}(p + F_{\mathrm{p}}n_{\mathrm{i}})} \tag{3.8}$$

$$F_{\mathrm{n}} = \frac{n}{N_{\mathrm{C}}} \exp\left(\frac{E_{\mathrm{C}} - E_{\mathrm{fn}}}{kT}\right) \tag{3.9}$$

$$F_{\mathrm{p}} = \frac{p}{N_{\mathrm{V}}} \exp\left(\frac{E_{\mathrm{fp}} - E_{\mathrm{V}}}{kT}\right) \tag{3.10}$$

where F_{n} and F_{p} are Fermi Dirac correction factors, and τ_{n}, τ_{p} are the electron and hole lifetimes. The same formulas are used for SRH generation, for which the sign of R_{SRH} is negative. Equation 3.8 has been simplified by assuming that the trap energy level is the intrinsic level, for which SRH is highest.

Experimental results in literature have shown the electron and hole lifetimes τ_{n} and τ_{p} are dopant-dependent [91]. In sentaurus Devices, the lifetimes are modeled with the empirical Scharfetter relation [91].

$$\tau = \frac{\tau_0}{1 + (N_{\mathrm{tot}}/N_{\mathrm{ref}})^{\gamma}} \tag{3.11}$$

where N_{tot} is the total doping concentration. N_{ref} is a reference doping concentration, and we choose $N_{\mathrm{ref}}{=}1 \times 10^{16}\,\mathrm{cm}^{-3}$, lower than the minimum doping concentration in our samples. γ is the dopant dependency exponent, and values between 0 and 2 have been reported for Silicon [91, 92]. By choosing $\gamma{>}0$, we assume the doping is purely dopant-induced. This assumption will be verified and confirmed later. Since we are unable to separate SRH generation of both minority carrier types, we assume $\tau{=}\tau_{\mathrm{n}}{=}\tau_{\mathrm{p}}$. The final assumption is that τ is temperature independent in the temperature range of the calibration. This will also be verified and confirmed later.

3.7.3 Lifetime calibration

We start by calibrating SRH for $T_{\mathrm{i}}{=}0\,\mathrm{nm}$. The dopant profile of this diode was not measured using SIMS, so we generate it from $T_{\mathrm{i}}{=}9\,\mathrm{nm}$, and we shift the Beryllium profile by an additional 9 nm as shown in figure 3.5(d) on p. 65. We then obtain a nearly constant total dopant concentration of $N_{\mathrm{tot}}{=}N_{\mathrm{Si}}{+}N_{\mathrm{Be}}{=}2 \times 10^{19}\,\mathrm{cm}^{-3}$. We consider the Jain-Roulston doping-dependent bandgap narrowing model discussed in section 2.2.4, which reduces the bandgap from 0.74 eV to 0.67 eV in the p+ region and 0.60 eV in

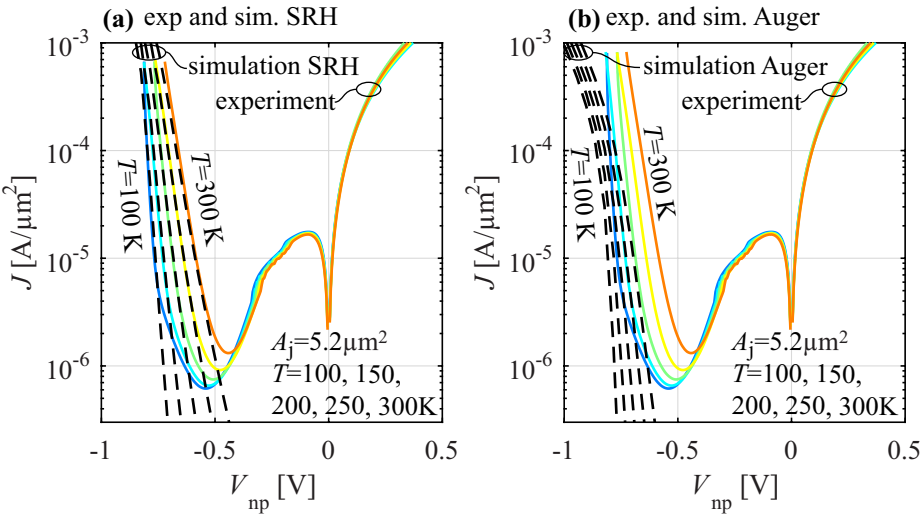


Figure 3.11: (a) For T_i=0 nm with N_tot=2 × 10^{19} cm^{-3}, SRH simulations and experiments match for τ=3 ps. (b) We verify the possibility of Auger instead of SRH recombination at high foward bias, but we do not obtain a agreement for voltage and temperature dependence.

the n+ region. We also include the temperature dependent bandgap narrowing model discussed in section 2.3.1, because we calibrate SRH at T=100 K and 300 K simultaneously. The minimum simulation temperature is 100 K due to convergence problems.

In a first step, we calibrate $\tau_\mathrm{n,p}$ while assuming a dopant independent lifetime (γ=0), because the total doping concentration is constant in this diode. Figure 3.11(a) shows we obtain a good match for T=100, 150, 200, 250 and 300 K using τ=3 ps. The match for all temperatures confirms our assumption of temperature independent lifetime.

In a second step, we investigate the dopant dependency exponent γ in the Scharfetter relation (equation (3.11) on p. 76). We verify whether γ is closer to 0, 1, or 2 by using the p+/i/n+ diodes with T_i=9 nm, 18 nm and 46 nm. For T_i=9, 18 nm we measure either dominant surface TAT/SRH or dominant BTBT, which means the simulated bulk SRH current should be below the measured current. For T_i=46 nm, temperature dependent I-V in figure 3.3(f) on p. 60 shows dominant SRH in forward bias and dominant BTBT in reverse bias. Since we cannot confirm the area scaling of SRH, we impose the condition that in reverse bias the simulated SRH current must be lower than the measured

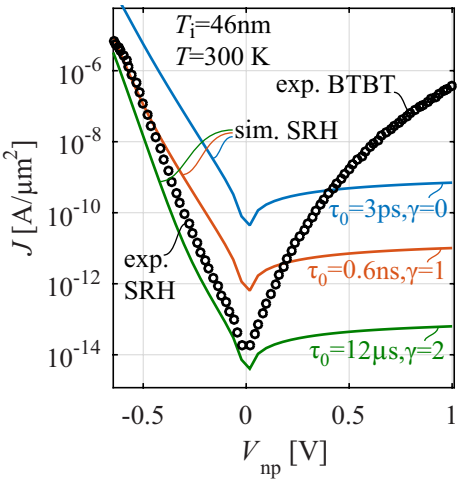


Figure 3.12: For T_i=46 nm in reverse bias, the simulated SRH current must be lower than the measured BTBT current. This confirms the lifetime is dopant dependent with $\gamma \geq 2$.

BTBT current.

We perform SRH simulations for T_i=9, 18, 46 nm using γ=0, 1, and 2 for the Scharfetter lifetime dependence. For every γ, we choose τ_0 to obtain τ=3 ps at $N_{tot}=2 \times 10^{19}\,cm^{-3}$. Figure 3.12 shows the simulated SRH for T_i=46 nm is lower than the measured current only for $\gamma \geq 2$. We obtain the same result for T_i=9 nm, 18 nm. Therefore, we conclude the lifetime has a inverse quadratic doping dependence.

3.7.4 Discussion

Fossum *et al.* analyzed the inverse quadratic doping dependence of the lifetime in Silicon [92], and suggested this could be caused by divacancy defects, each causing two trap energy levels. This results in a trap density (N_t) which increases quadratically with doping concentration.

From equation 3.8 on p. 76 we see that for forward bias ($p \times n \gg n_i^2$), SRH is highest where the $p \times n$ product is highest. Simulations of the forward biased p+/n+ diode show this happens at the p+ side of the p+/n+ junction, because the minority carrier concentration is much higher there than at the n+ side, due to the lower Fermi level degeneracy. The dopant-induced SRH is therefore generated by Beryllium atoms with $N_{Be}=2 \times 10^{19}\,cm^{-3}$.

In reverse bias ($p \times n \ll n_i^2$), SRH generation is uniform in the whole depletion region due to the low carrier concentration. In the depletion region, figure 3.5(b) on p. 65 shows the Beryllium background concentration is N_{Be}=$2 \times 10^{17}\,cm^{-3}$, and previous measurements of Silicon background concentrations in the MBE show N_{Si}=$1 \times 10^{16}\,cm^{-3}$. This also indicates that the dopant-induced SRH is generated by Beryllium atoms. We conclude that the SRH carrier lifetime is temperature independent and has the form

$$\tau_n = \tau_p = \frac{12\mu s}{1 + (N_{Be}/10^{16}cm^{-3})^2} \tag{3.12}$$

Instead of SRH recombination, Fossum *et al.* also identified two alternative recombination mechanism at high free carrier density [92]. The first possibility is Auger recombination, simulated in figure 3.11(b). Auger recombination is commonly associated with a lifetime which is inversely quadratic with the majority carrier concentration, because the energy released by the electron-hole pair recombination is absorbed by a third particle, a free electron or hole [29, p. 66]. For $In_{0.53}Ga_{0.47}As$ with a doping level of $2 \times 10^{19}\,cm^{-3}$, electron and hole lifetimes of 50 ps [93] and 20 ps [94] have been measured optically. These are longer than our value of 3 ps, indicating that Auger recombination is probably not dominant in our diodes. In figure 3.11(b), we perform simulations of the Auger recombination current with input parameters from literature [94], and we obtain an ideality factor of 1 at all temperatures. However, our measurements show an ideality factor of 1.2, which is typical for SRH. We conclude Auger recombination is not dominant in our diodes.

Fossum *et al.* also proposed the possibility of trap-assisted Auger recombination as a possibility for the inverse quadratic doping dependence of the lifetime [92]. The process is similar to SRH, but the recombination energy is given to a free electron/hole in case of Auger, instead of a phonon in case of SRH. Unfortunately, the quadratic dependence of trap-assisted Auger recombination cannot be modeled with Sentaurus Device. We suggest verifying this in future work. We are confident with the SRH model in figure 3.11(a), since we obtain excellent agreement between the experiments and the simulated SRH current, for the temperature dependence as well as the voltage dependence. For the remainder of this chapter, we assume dominant SRH recombination at high forward bias, instead of trap-assisted Auger recombination. This is a worst-case scenario for the extrapolation to generation current in the TFET, because dopant-induced SRH generation is likely higher than the reverse process of Auger recombination, which is impact ionization. Impact ionization requires free carriers with a high kinetic energy, which are absent in TFETs with low operating voltage and small dimensions. Therefore impact ionization is negligible in TFET and our calibration is a worst-case scenario.

3.8 TAT calibration

3.8.1 Analysis of electrical results

For T_{i}=0 nm, figure 3.3(a) on p. 60 shows that below T=100 K, there is an additional TAT current component in forward bias. It is nearly temperature independent for T<100 K. This temperature independence was also observed in other work on Germanium Esaki diodes [77]. We attribute this to the electron and hole densities at the start and end of the tunnel path which are nearly constant with temperature. Figure 3.4(a) shows the TAT current scales with the junction area, which means it's a bulk property of $In_{0.53}Ga_{0.47}As$ and its epitaxial growth. We will therefore calibrate the TAT model using this data, so we can apply it to TFET simulations.

For T_{i}=9 nm, 18 nm at large forward bias, we extract an inverse slope of 180 mV/dec, constant with temperature, which also suggests TAT recombination [73]. Figures 3.4(c) and 3.4(d) for T=4 K and 300 K show that TAT scales with the square root of the diode area, which is equivalent to the diode perimeter. Therefore the TAT current is related to the unoptimized sidewall wet etching process, and it is therefore not useful to calibrate it.

3.8.2 Schenk nonlocal TAT model and assumptions

In Sentaurus Device's implementation of the "Dynamic nonlocal path TAT" model, electrons and holes are captured in or emitted from a defect by phonon-assisted tunneling. This results in three different position-dependent generation/recombination rates: the electron capture in the conduction band, the hole capture in the valence band, and the recombination of both carriers at the defect level. These three recombination rates are shown in figure 3.13(b) for the p+/n+ diode under forward bias.

The first input parameters for the TAT model are the tunneling parameters A_{BTBT}, B_{BTBT}, which are known from the BTBT calibration in section 3.5.2. To include the phonon-assisted process, we provide as input parameters the $In_{0.53}Ga_{0.47}As$ longitudinal optical phonon energy $\hbar\omega$=34 meV, which we obtain from literature [48]. Other input parameters are the Huang-Rys factor S, which is a measure for the electron-phonon coupling, the carrier lifetimes $\tau_{\mathrm{n,p}}$ and finally the trap energy level E_{t}.

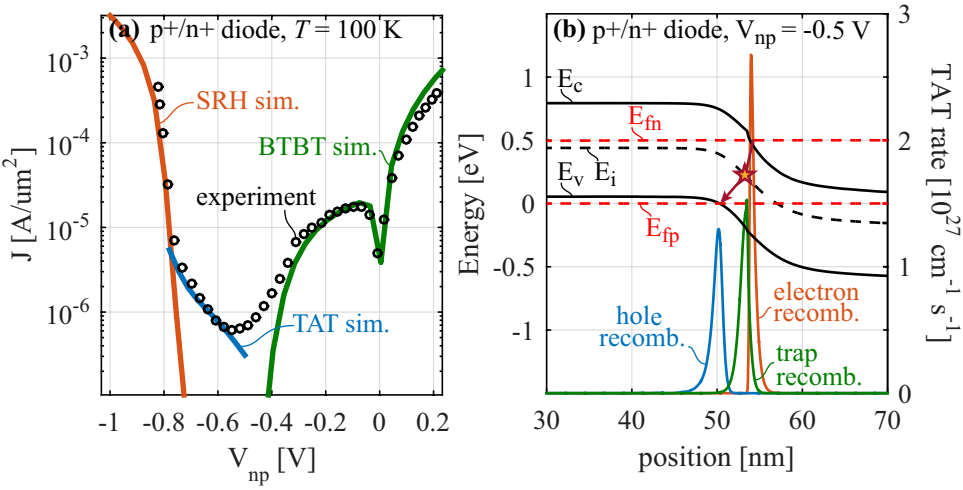


Figure 3.13: (a) For the p+/n+ diode, we obtain a good match between experiments and simulated TAT using S=10 and τ=0.7 ns. The calibrated SRH and BTBT from sections 3.5.2 and 3.5.2 is also shown. (b) The TAT recombination process is modeled as three processes at a different location and energy: an electron capture in the conduction band, a hole capture in the valence band, and the recombination of both carriers at the defect (star symbol).

3.8.3 Calibration

We then calibrate the parameters S and τ, while assuming τ=τ_n=τ_p, and E_t=E_i. The possible error for the last assumption will be verified later. The calibration is performed at T=100 K, because at room temperature the measured SRH is dominant over the measured TAT. At T=4 K the simulations do not converge.

From simulations we observe that a change in the Huang-Rys coupling factor S changes the slope of the TAT I-V curve, but a decrease of the carrier lifetime τ increases the current equally at all voltages. We can therefore decouple both parameters and we obtain a single solution for the calibration, using S=10 and τ=0.7 ns. This lifetime is valid for a doping concentration of N_{tot}=2×10^{19} cm^{-3} and assuming E_t=E_i. Figure 3.13(a) shows the calibrated TAT current, together with the calibrated SRH current from section 3.7 and a BTBT simulation using the calibrated parameters from section 3.5.2.

We verify the impact of the assumption E_t=E_i. For the SRH process, the generation/recombination current is highest when the trap level is located at

midgap, but this is different for the TAT process. In case of TAT generation, a bound electron is first excited from the valence band to the defect state in the bandgap, then in a second step from the defect to the conduction band, all by a combination of thermal steps and tunneling steps. Unlike SRH, the efficiency is typically highest for defect energy levels at 1/3 or 2/3 of the bandgap [87]. To assess the impact of the defect energy level on the TAT generation rate, we perform additional TAT calibrations with E_t located at E_i-0.2 eV, E_i-0.1 eV, E_i+0.1 eV, E_i+0.2 eV. We determine that the unknown value of E_t causes an uncertainty of a factor 3 on the TAT generation current in reverse bias. This factor 3 is sufficiently low to make conclusions about TAT in TFETs in the following section.

In conclusion, we have calibrated the TAT model in Sentaurus device using p+/n+ $In_{0.53}Ga_{0.47}As$ diodes which have a total dopant concentration $N_{tot}=2 \times 10^{19}\,cm^{-3}$. The TAT current is dominant only at $T \leq 100\,K$, because SRH is dominant at higher temperatures. We obtain the input parameters S=10 and τ=0.7 ns when assuming $E_t=E_i$. When relaxing this assumption, we can predict the TAT generation rate in diodes and TFETs with an uncertainty factor of 3.

3.9 InGaAs TFET performance prediction

In this section, we predict the transfer characteristics of $In_{0.53}Ga_{0.47}As$ homojunction TFETs. The first set of simulations are for an n-type point-TFET, introduced in section 1.4. We perform these simulations with the Sentaurus Device [27] with the following models:

- Fermi-Dirac statistics and multivalley band structure with nonparabolic correction introduced in section 2.2.2
- bulk SRH model with calibrated values from section 3.7
- Schenk nonlocal TAT model with calibrated values from section 3.8
- nonlocal BTBT model with recommended calibrated values from table 3.1

The goal of these first simulations is to understand where bulk TAT and SRH occur and how to suppress it. The second set of simulations are for more advanced pocketed line-TFET configuration. We simulate the BTBT current only, but for both the n-type and p-type TFETs. We compare the performance of these line-TFETs to Silicon MOSFET for a supply voltage of V_{dd}=0.5 V.

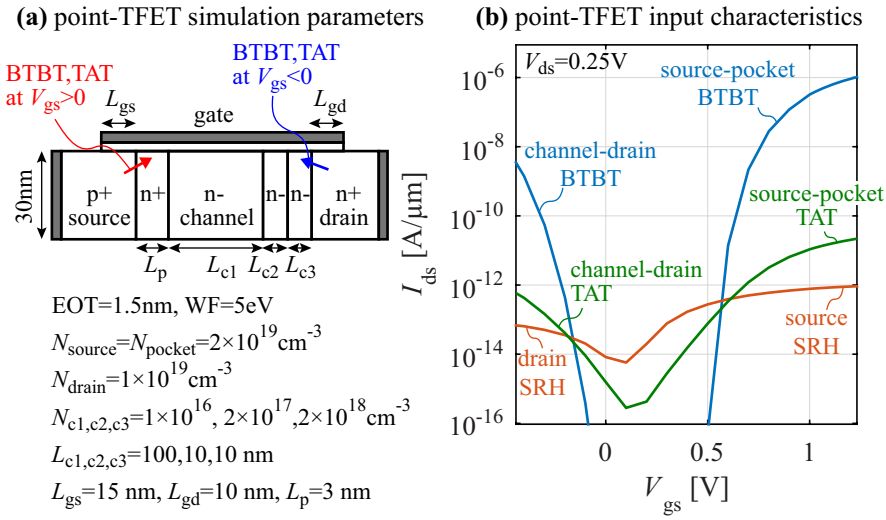


Figure 3.14: (a) We simulate BTBT, SRH and TAT in a n-type point-TFET with n+ pocket with $V_{ds} = 0.25\,V$. The gate overlaps the source and drain regions, which is common for fabricated TFETs in literature. (b) The transfer characteristics show BTBT, TAT, and SRH each have two branches due to generation in either the source or the drain region.

3.9.1 Point-TFET simulation

The point-TFET configuration is shown in figure 3.14(a). It features a 3 nm n+ pocket between the source and the channel to increase I_{on}, and a gradual increase of channel doping at the drain side over 20 nm to decrease ambipolar BTBT. The gate stack overlaps the highly doped source and drain regions with lengths L_{gs} and L_{gd}. A gate overlap is common for TFETs in literature [76, 18, 21] because this relaxes the gate alignment requirement. We assume the n-type dopants in the pocket and drain regions have the same impact on the SRH lifetime as Beryllium dopants. TAT and SRH due to interface defects are not calibrated and therefore not included.

The simulated transfer characteristics are shown in figure 3.14(b). The BTBT generation features two branches, one for more positive V_{gs} due to electron tunneling at the source-pocket junction (red arrow), and the ambipolar branch for more negative V_{gs} due to hole tunneling at the drain/channel junction (blue arrow). The ambipolar branch is strongly suppressed by the gradually increasing dopant concentration at the drain/channel junction. The TAT current is composed of two branches similar to the BTBT current, which is expected

because TAT is electric field-assisted. The ambipolar BTBT and TAT currents increase with V_{ds}, because this increases the electric field at the channel/drain junction.

For the V_{gs} dependence of SRH, we obtain a surprising result. It is commonly assumed SRH is generated in the depleted region of the reverse biased p+/i/n+ diode [76, 95], and is nearly independent on V_{gs} because SRH is not field-assisted. In our case, SRH is dominant over TAT in the TFET off-state, SRH is gate bias dependent and also consists of two branches. For more positive V_{gs}, SRH generation occurs mainly in the depleted n+ pocket and in the depleted p+ source region directly underneath the gate. For more negative V_{gd}, SRH generation happens in the depleted n+ drain region directly underneath the gate and scales with L_{gd}.

This can be understood from equation (3.8). SRH generation is high in locations where $p \times n \ll n_i^2$, and where $\tau_{n,p}$ is low. These conditions are satisfied in the aforementioned regions, because the SRH lifetime has an inverse quadratic doping dependence. SRH in the lowly doped channel region is at least $10^4\times$ lower than in the other highly doped regions. Therefore, when fabricating and optimizing a TFET, scaling down L_{gd} and especially L_{gs} will lead to a larger decrease in bulk SRH leakage, than scaling down the channel length L_c.

We also observe from figure 3.14(b) that the amount of SRH and TAT generation due to bulk defects is rather low. In the region $0\,\text{V}<V_{gs}<0.5\,\text{V}$, SRH and TAT are larger than BTBT, but are less than $1\,\text{pA}\,\mu\text{m}^{-1}$, which is negligible compared to the target off-state current of $50\,\text{pA}\,\mu\text{m}^{-1}$ (defined in section 1.3). If we generally apply this conclusion to lattice matched $In_{0.53}Ga_{0.47}As$ TFET with similar doping concentrations, the bulk semiconductor defects not problematic for the TFET performance. More significant problems are expected from defects at the semiconductor/oxide interface, and at the hetero-interface in heterojunction TFET. Therefore we recommend calibrating SRH and TAT due to interface defects in future work. Avci *et al.* made a similar conclusion about Germanium TFET [85]. Avci calibrated the bulk BTBT, SRH and TAT models using Germanium p+/i/n+ diodes and observed that the bulk SRH and TAT currents are sufficiently low.

3.9.2 Line-TFET simulations

The second configuration is a line-TFET, where the gate covers the source and a counterdoped pocket (inset figure 3.15). This results in tunneling perpendicular to the gate. After the tunneling event, the charge carrier flows underneath the gate dielectric towards the drain. Because the tunneling is uniform over the

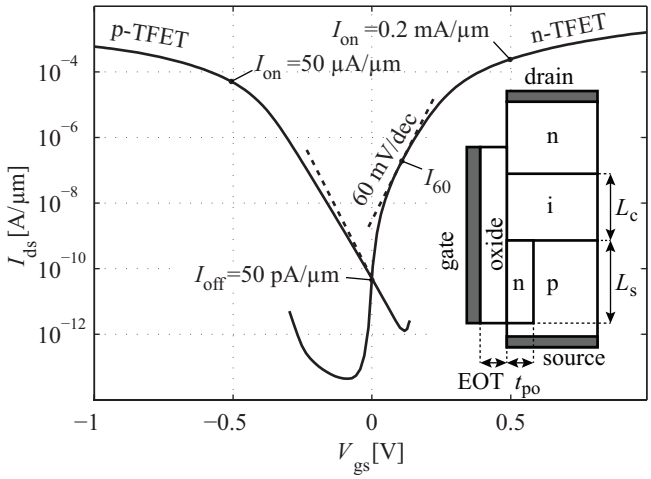


Figure 3.15: The transfer characteristics are shown for n-lineTFET (inset) and p-lineTFET. For n-TFET, t_{po}=3 nm and the gate workfunction WF=4 eV. The source and pocket dopant concentrations are N_s=N_p=1×10^{20} cm^{-3}. For p-TFET, t_{po}=5 nm, WF=5 eV, all dopant types shown in the inset are reversed and N_s=N_p=5×10^{19} cm^{-3}. For both TFET, EOT=0.6 nm and the drain voltage is V_{ds}=0.5 V. The source and channel length are L_s=30 nm and L_c=50 nm, respectively.

whole source-pocket junction, this configuration provides a steeper subthreshold swing compared to point-TFET [11, 10].

The semi-classical simulator does not consider Field-Induced Quantum Confinement (FIQC). According to QM simulations [65], FIQC results in a delayed onset of BTBT due to quantized energy levels in the source near the gate. Therefore, FIQC results in shifted transfer characteristics and a slightly lower on-current, especially for line-TFET. In chapter 5, we experimentally confirm the delayed onset of BTBT.

The n-type TFET has a sub-60 mV/dec subthreshold swing, and the transition point [7] from sub-60 mV/dec to super-60 mV/dec is I_{60}=0.2 µA µm^{-1}. Compared to MOSFET [6], the pocketed $In_{0.53}Ga_{0.47}As$ n-lineTFET shows competitive performance with I_{on}=0.2 mA µm^{-1} in a supply voltage window V_{dd}=0.5 V.

The pocketed p-type line-TFET does not reach a sub-60 mV/dec subthreshold swing. This is expected, because the high source doping concentration and low conduction band density of states cause a high Fermi level degeneracy in the

source. This negatively impacts the energy filtering mechanism of the p-TFET [96].

In other work, Verreck *et al.* have performed QM p-TFET simulations using the calibrated parameters from section 3.6, and have proposed an improved lowly doped source design to recover the energy filtering mechanism [97]. They demonstrate similar p-TFET and n-TFET performance, despite the low conduction band density of states. The $In_{0.53}Ga_{0.47}As$ p-TFET shows promising performance with I_{60}=2 µA µm^{-1} and I_{on}=320 µA µm^{-1} at V_{dd}=0.5 V using calibrated QM simulations.

3.10 Conclusions

We calibrated BTBT for a semi-classical simulator and a QM simulator using $In_{0.53}Ga_{0.47}As$ p+/i/n+ diodes. The recommended input parameters are $A_{BTBT} = 1.3 \times 10^{20}\,cm^{-3}s^{-1}$, $B_{BTBT} = 5.7 \times 10^{6}\,Vcm^{-1}$ for the former, and $E_P = 15\,eV$ for the latter. This value of E_P correctly describes BTBT, unlike values recommended for $\mathbf{k} \cdot \mathbf{p}$ implementations with perturbative inclusion of higher bands. We determined the uncertainty on the BTBT rate, resulting in ±30% at electric fields typical for TFET, and ±50% at electric fields typical for MOSFET. This low uncertainty was accomplished by determining the dopant profile with complementary SIMS and *C-V* measurements. The range of calibrated parameters encompasses the theoretically predicted values, confirming the validity of direct BTBT models for $In_{0.53}Ga_{0.47}As$. Our result suggests that reliable predictions can be made for other direct bandgap materials with the existing model. This work was published in *Journal of Applied Physics* in 2014 [98].

We also calibrated bulk SRH and bulk TAT models for the semi-classical simulator using $In_{0.53}Ga_{0.47}As$ p+/n+ diodes. In future work, the exclusion of trap-assisted Auger recombination needs to be confirmed. We applied the SRH and TAT models to simulations of $In_{0.53}Ga_{0.47}As$ homojunction point-TFET where the gate overlaps the source and drain regions. We conclude SRH is dominant in the off-state and gate bias dependent, because SRH generation happens mainly in the depleted gate/source and gate/drain overlap regions. For a source and drain doping concentration of $2 \times 10^{19}\,cm^{-3}$, reducing these overlap lengths to less than 500 nm is sufficient to suppress the SRH current to <50 pA µm^{-1}. Generally, for lattice matched $In_{0.53}Ga_{0.47}As$ TFET with source/drain doping concentrations near N=$2 \times 10^{19}\,cm^{-3}$ and gate/source and gate/drain overlap regions less than 500 nm, the contributions of SRH and TAT generation due to bulk defects are negligible, even when considering the

uncertainty about trap-assisted Auger recombination. Therefore it is likely that the SRH and TAT current observed in experimental lattice matched TFET in literature [21] is caused by interface defects.

We have also predicted the transfer characteristics of more advanced n-type and p-type $In_{0.53}Ga_{0.47}As$ homojunction line-TFET using the calibrated semi-classical simulator. Compared to Silicon MOSFET, the nTFET shows competitive performance with I_{on}=0.2 mA µm^{-1} at V_{dd}=0.5 V. Similar pTFET characteristics can be achieved using a lowly doped source design.

Chapter 4

Extracting the band alignment of heterojunctions

The effective bandgap for heterojunction tunneling ($E_{g,eff}$) is a crucial design parameter of heterojunction TFET. However, there is still significant uncertainty on $E_{g,eff}$ for the $GaAs_{0.5}Sb_{0.5}/In_{0.53}Ga_{0.47}As$ heterojunction.

In section 4.1, we demonstrate using quantum mechanical simulations how $E_{g,eff}$ affects key performance metrics in a $GaAs_{0.5}Sb_{0.5}/In_{0.53}Ga_{0.47}As$ TFET. In section 4.2, we calibrate $E_{g,eff}$ for this heterojunction. We achieve this by comparing the simulated and measured I-V and C-V characteristics of p+/i/n+ heterojunction diodes. We use the calibrated BTBT parameters from chapter 3, and we take $E_{g,eff}$ as a fitting parameter. For these diodes, BTBT occurs in the nearly intrinsic region which is not affected by Dopant-dependent Bandgap Narrowing (DOPBGN). In section 4.3, we focus on n++$In_{0.53}Ga_{0.47}As$/p+$GaAs_{0.5}Sb_{0.5}$ Esaki diodes, where BTBT occurs in heavily doped regions. The impact of DOPBGN on the BTBT rate is not well known, therefore we extract $E_{g,eff}$ with an alternative method. The method is based on an unusual exponentially increasing current with forward bias, caused by sharp energy filtering at cryogenic temperature. The method does not require the BTBT rate, but it does require knowledge of the electrostatic potential profile. Finally, we compare the values of $E_{g,eff}$ obtained using both methods in the discussion (section 4.3.6).

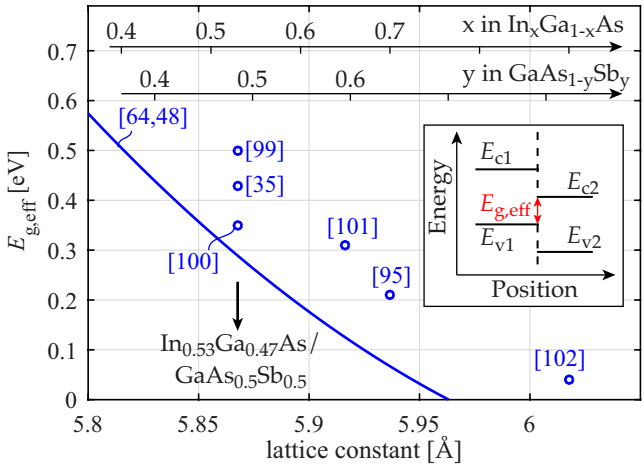


Figure 4.1: Many lattice matched $In_xGa_{1-x}As/GaAs_{1-y}Sb_y$ heterojunction TFETs have been demonstrated in literature, but there is significant uncertainty on the reported $E_{g,eff}$. The circles are the reported values in the respective papers, and the full line is calculated from electron affinities [48] and bandgaps [64] of the bulk materials. The value for [100] was measured at T=10 K with photoluminescence and we extrapolated it to T=300 K using temperature-dependent bandgap narrowing data [71, 103].

4.1 Impact of the effective bandgap on heterojunction TFET

The effective bandgap at the tunneling junction ($E_{g,eff}$, inset figure 4.1) is a crucial design parameter for heterojunction TFET. The lattice-matched $In_xGa_{1-x}As/GaAs_{1-y}Sb_y$ heterojunction system is promising for TFET [99, 35, 48, 19, 100, 101, 95, 102, 64] due to its tunable $E_{g,eff}$. Figure 4.1 shows $E_{g,eff}$ decreases with increasing lattice constant, which is achieved by changing the compositions x and y.

$E_{g,eff}$ is usually determined from the electron affinities [48] and bandgaps [64] of the bulk materials (full line in figure 4.1), or using optical measurements [19, 100, 104, 105]. However, there is significant uncertainty on $E_{g,eff}$, especially for the combination $In_{0.53}Ga_{0.47}As/GaAs_{0.5}Sb_{0.5}$ which is popular due to its lattice matching with InP substrates. This uncertainty on $E_{g,eff}$ makes the prediction of TFET performance difficult. Quantum Mechanical (QM) simulations of an $In_{0.53}Ga_{0.47}As/GaAs_{0.5}Sb_{0.5}$ TFET in figure 4.2 show $E_{g,eff}$ has a strong impact on I_{on} and I_{60} (introduced in section 1.3 on p. 10). When $E_{g,eff}$ decreases

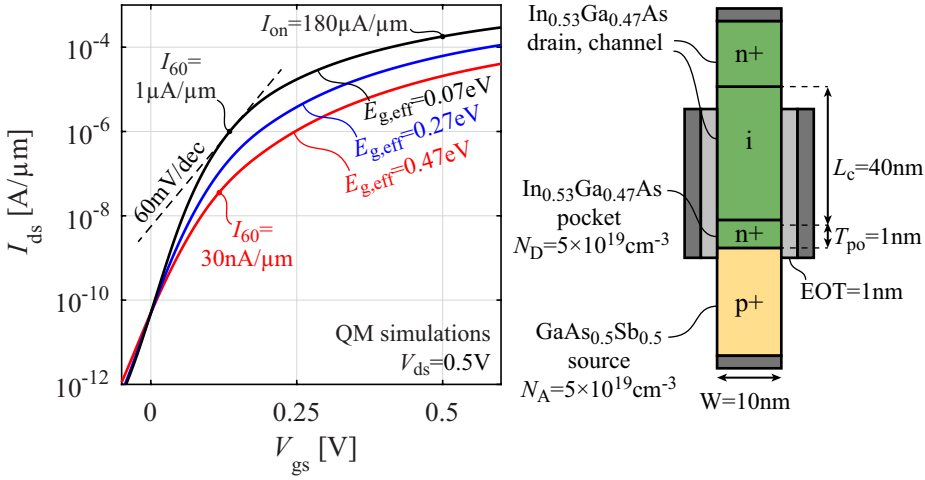


Figure 4.2: $In_{0.53}Ga_{0.47}As/GaAs_{0.5}Sb_{0.5}$ TFET simulations with a 15-band k.p solver (introduced in section 2.2.6) show $E_{g,eff}$ significantly impacts I_{60} and I_{on}. The $In_{0.53}Ga_{0.47}As$ electron affinity is artificially changed to obtain different $E_{g,eff}$.

from 0.47 to 0.27 eV, I_{60} increases by a factor 6. Therefore we have designed experiments to calibrate $E_{g,eff}$ and decrease this uncertainty.

4.2 Calibrating the effective bandgap in p+/i/i/n+ hetero-diodes

In this section, we fabricate heterojunction diodes and we compare the simulated and the measured I-V and C-V curves. We calibrate $E_{g,eff}$ by taking it as a fitting parameter. This approach is valid because the BTBT parameters for $In_{0.53}Ga_{0.47}As$ are already known from the calibration in chapter 3, and are close to the values from Kane's theory (table 3.1 on p. 71). Therefore, we expect the BTBT parameters for $GaAs_{0.5}Sb_{0.5}$ are similarly close to the values predicted by theory.

We calibrate $E_{g,eff}$ using p+/i/n+ diodes, where the heterojunction is located in the middle of the intrinsic region. We therefore call these p+/i/i/n+ diodes, where the first two regions are $GaAs_{0.5}Sb_{0.5}$ and the last two regions are $In_{0.53}Ga_{0.47}As$. For these diodes, the tunneling paths are mainly located in the intrinsic regions, which is less affected by Dopant-dependent Bandgap

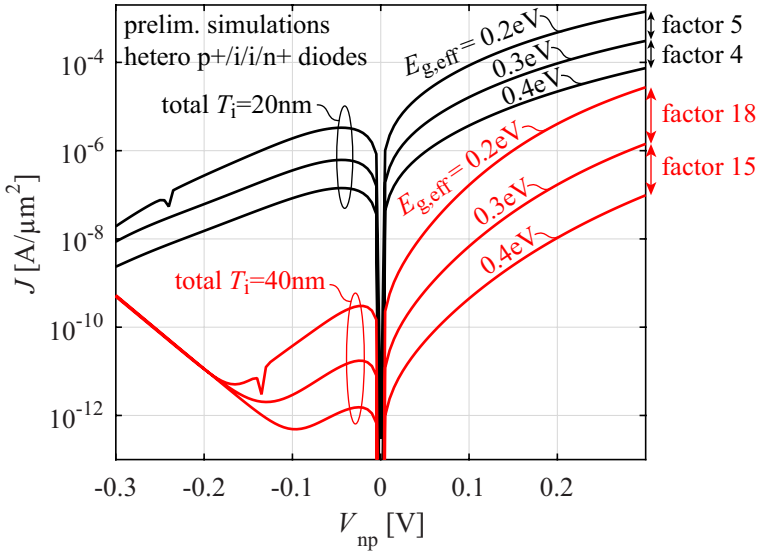


Figure 4.3: Preliminary Sentaurus Device [27] simulations of $GaAs_{0.5}Sb_{0.5}$/ $In_{0.53}Ga_{0.47}As$ p+/i/i/n+ diodes show the BTBT current is more sensitive to $E_{g,eff}$ in case of T_i=40 nm compared to T_i=20 nm. We apply box dopant profiles with target N_D=N_A=2×10^{19} cm^{-3} in the highly doped regions.

Narrowing (DOPBGN). Note that we avoid performing the calibration using p+/n+ heterojunction diodes, because the tunnel paths would be located in a region affected by DOPBGN. The impact of DOPBGN on the BTBT rate is not well known.

4.2.1 Choice of intrinsic region thickness

We perform preliminary simulations to design the p+/i/i/n+ diodes and choose an appropriate total intrinsic region thickness T_i to achieve a high measurement sensitivity to $E_{g,eff}$. Figure 4.3 shows I_{BTBT} is more sensitive to $E_{g,eff}$ when choosing a larger T_i. When using T_i=20 nm, I_{BTBT} at V_{np}=0.5V increases by a factor 4-5 for every 0.1 eV decrease in $E_{g,eff}$. When using T_i=40 nm, the current increases by a factor 15-18 for every 0.1 eV decrease in $E_{g,eff}$. The sensitivity of the latter is sufficiently high to reduce the uncertainty on $E_{g,eff}$ compared to literature, where a range $E_{g,eff}$=0.29 − 0.5 eV is found (figure 4.1).

The sensitivity of I_{BTBT} to $E_{g,eff}$ is related to the built-in electric field at V_{np}=0 V (F_{bi}) in the p+/i/i/n+ diode. When T_i is longer, F_{bi} is lower, and a

small change in $E_{g,eff}$ will have a larger impact on I_{BTBT}. This is intuitively understood from Kane's BTBT rate equation, valid for a semiconductor in a uniform electric field F (equation (2.1) on p. 25) and plotted in figure 2.3 on p. 27. This figure shows G_{BTBT} changes rapidly with F when $F \ll B_{BTBT}$, but the change is only quadratic when $F \gg B_{BTBT}$. For $In_{0.53}Ga_{0.47}As$ or $GaAs_{0.5}Sb_{0.5}$, $B_{BTBT} \approx 6$ MV/cm. Therefore, for the heterojunction diodes, we target $T_i = 40$ nm to have $F_{bi} \approx 0.1$ MV/cm. As a result, a small variation in $E_{g,eff}$ induces a large change of I_{BTBT}.

4.2.2 Diode fabrication

A stack with target specifications 600 nm p+$GaAs_{0.5}Sb_{0.5}$/ 20 nm undoped $GaAs_{0.5}Sb_{0.5}$/ 20 nm undoped $In_{0.53}Ga_{0.47}As$/ 50 nm n+$In_{0.53}Ga_{0.47}As$ is epitaxially grown on a p-type InP substrate by Molecular Beam Epitaxy (MBE). The growth technique is described in ref. [106]. The target dopant concentrations for the highly doped regions are $N_A = N_D = 2 \times 10^{19}\,cm^{-3}$. The InP substrate doping concentration is $N_A = 5 \times 10^{17}\,cm^{-3}$, and the substrate orientation is such that tunneling occurs in the [001] direction.

With this stack, we fabricate diodes according to the process flow in figures C.1-C.2 on p. 179-180. All details are in appendix C, but we provide a brief summary here. After the epitaxial growth, we define the diode shapes with junction areas 0.01-215 µm^2 using flowable oxide (FOx12) and e-beam. We then apply a 30 nm AuZn/70 nm Au contact to the back side of the InP substrate and anneal it during 5 min at 400°C. The diode mesas are wet etched using a diluted citric acid/peroxide solution. A 2.8 µm thick Benzocyclobutene dielectric (BCB3022-46) is spun on the diodes, cured, and recessed using O_2/SF_6 Reactive Ion Etching (RIE) until the FOx12 is exposed. The FOx12 is wet etched using a buffered HF solution, which also removes the $In_{0.53}Ga_{0.47}As$ native oxide, and we immediately deposit a 20 nm Mo/150 nm Au metal stack by sputtering. Contact pads are defined using a bilayer i-line resist stack of LOR1A/IX845 and Xenon Ion milling. The bilayer resist stack is removed using a MS2001 microstrip solution, and the exposed BCB is recessed using O_2/SF_6 RIE.

4.2.3 Electrical characterization

The I-V characteristics are corrected for series resistance (R_s). R_s is extracted from the exponentially increasing current at high forward bias, as discussed in section 3.3.1 on p.57. We obtain values for R_s between 620 Ω for $A_j = 0.01$ µm^2 and 330 Ω for $A_j = 215$ µm^2.

We analyze the temperature dependent I-V characteristics of a diode with A_j=9.2 µm^2 in figure 4.4(a). For a reverse bias voltage V_{np}>0.2 V, the activation energy near room temperature is E_a=0.04 eV and nearly constant in the range V_{np}>0.2 V. This small temperature dependence indicates dominant BTBT. Figures 4.4(c-d) show the BTBT current in reverse bias scales with the tunnel junction area A_j.

In the voltage range $-1\,V<V_{np}<0.2\,V$, the current has a larger temperature dependence with an activation energy E_a=0.1−0.2 eV near room temperature. As discussed in section 2.3.6 on p. 42, this suggests TAT [75, 73]. This TAT current scales with $A_j^{1/2}$ (plot not shown), which is proportional with the perimeter of the diode, and indicates the TAT current is induced by defects at the diode sidewalls.

We obtain pure BTBT current by lowering the temperature to 77 K. Fig. 4.4(a) shows this suppresses TAT generation/recombination and reveals the BTBT component in forward bias, with the characteristic Negative Differential Resistance (NDR) region for $-0.1\,V<V_{np}<-0.05\,V$.

4.2.4 Extrapolating the pure BTBT current

In the coming paragraphs, we will extrapolate this pure BTBT current from T=77 K to T=300 K. This way we can calibrate $E_{g,eff}$ at room temperature, and over the largest possible V_{np} range.

We start by modeling the temperature dependence of the BTBT current. A first model is the activation energy method, which is convenient to distinguish BTBT from SRH and TAT processes. The temperature dependence of I_{BTBT} is modeled as

$$I_{BTBT} \propto \exp\left(\frac{-E_a}{k_B T}\right) \tag{4.1}$$

where k_B is the Boltzmann constant. However, this model does not really capture the physics of BTBT, since BTBT is not an Arrhenius process with a thermal activation step. This is reflected by an inconsistent activation energy over a wide range of temperatures, with E_a=0.04 eV near room temperature and E_a=0.002 eV near 77 K (both for V_{np}=0.2V).

To capture the temperature dependence of BTBT more accurately, we derive a model for homojunction BTBT based on Kane's theory [47] and Temperature-dependent Bandgap Narrowing (TBGN) introduced in section 2.3.1 on p.38. We consider Kane's BTBT rate equation for a single semiconductor

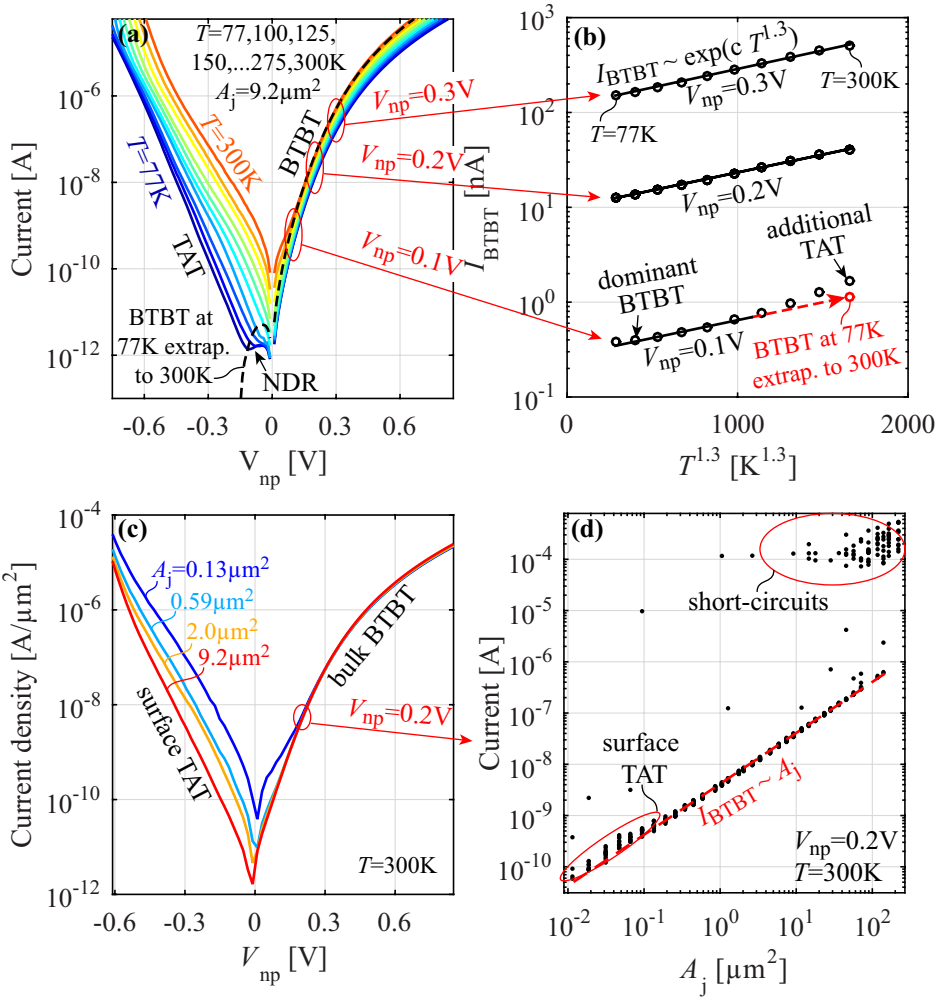


Figure 4.4: (a) By lowering the temperature from 300 to 77 K, TAT is suppressed and BTBT is dominant for $V_{\rm np}>-0.1$ V. The dashed line shows the BTBT current extrapolated from 77 to 300 K. (b) We fit the measured BTBT current (circles) to our model (lines) with $I_{\rm BTBT}\propto\exp(c\,T^{1.3})$. We obtain the same slope c for $V_{\rm np}$=0.1, 0.2, 0.3 V, allowing us to extrapolate for even smaller $V_{\rm np}$. (c-d) BTBT in reverse bias scales with the junction area $A_{\rm j}$ (bulk BTBT), but TAT in forward bias scales with the diode perimeter due to surface defects. The largest diodes are short-circuited due to a BCB recess issue.

with uniform electric field (section 2.2.1 on p.25):

$$I_{\mathrm{BTBT}} \propto G_{\mathrm{BTBT}} = \frac{g m_{\mathrm{r}}^{1/2} (qF)^2}{\pi h^2 \sqrt{E_{\mathrm{g}}}} \exp\left(\frac{-\pi^2 m_{\mathrm{r}}^{1/2} {E_{\mathrm{g}}}^{3/2}}{Fqh}\right) \tag{4.2}$$

where g is the degeneracy factor, m_{r} is the reduced tunnel mass, q is the elementary charge, F is the uniform electric field and h is Planck's constant. In the range T>77 K, the temperature dependence of the bandgap E_{g} of $In_{0.53}Ga_{0.47}As$ can be approximated by

$$E_{\mathrm{g}} \approx E_{\mathrm{g},0} - \alpha T \tag{4.3}$$

where α is an empirical fitting parameter [71]. When F is low ($F \ll B_{\mathrm{BTBT}}$), the exponential part of eq. (4.2) is the dominant contribution to the temperature dependence of I_{BTBT}. We evaluate eq. (4.2) for $In_{0.53}Ga_{0.47}As$ using the temperature dependence data in [71] and obtain

$$I_{\mathrm{BTBT}} \propto \exp\left(c\, T^{1.3}\right) \tag{4.4}$$

where c is a fitting parameter. The exponent $n = 1.3$ is obtained with a numerical fit in the temperature range T>77 K and low electric field limit ($F \ll B_{\mathrm{BTBT}}$). The temperature dependence BTBT in $GaAs_{0.5}Sb_{0.5}$ is similar [103].

We extrapolate this model for homojunction tunneling and apply it to our heterojunction experiments. In figure 4.4(b), we consider the experimentally measured current from T=77 to 300 K for V_{np}=0.1, 0.2 and 0.3 V. We apply eq. (4.4) to fit the experimental data and we obtain much better agreement with this model than with the activation energy model. The slope c of the temperature dependence is nearly identical for the three voltages. We now consider the I-V trace at T=77 K, where TAT is suppressed and BTBT is dominant in the range V_{np}>−0.1 V. We first subtract the TAT current in forward bias using an exponential fit line. We then extrapolate the full I-V trace to T=300 K, as shown for V_{np}=0.1 V by the dashed arrow in figure 4.4(b). Finally we obtain the dashed curve in figure 4.4(a), which is the extrapolated pure BTBT current at T=300 K. We will use this I-V trace for the calibration of $E_{\mathrm{g,eff}}$ in section 4.2.6.

4.2.5 C-V and SIMS characterization

We combine C-V and Secondary Ion Mass Spectrometry (SIMS) measurements to gain additional accuracy on the electrostatic profile in the simulations, as performed in section 3.4.5 on p. 68 for homojunction diodes. The C-V

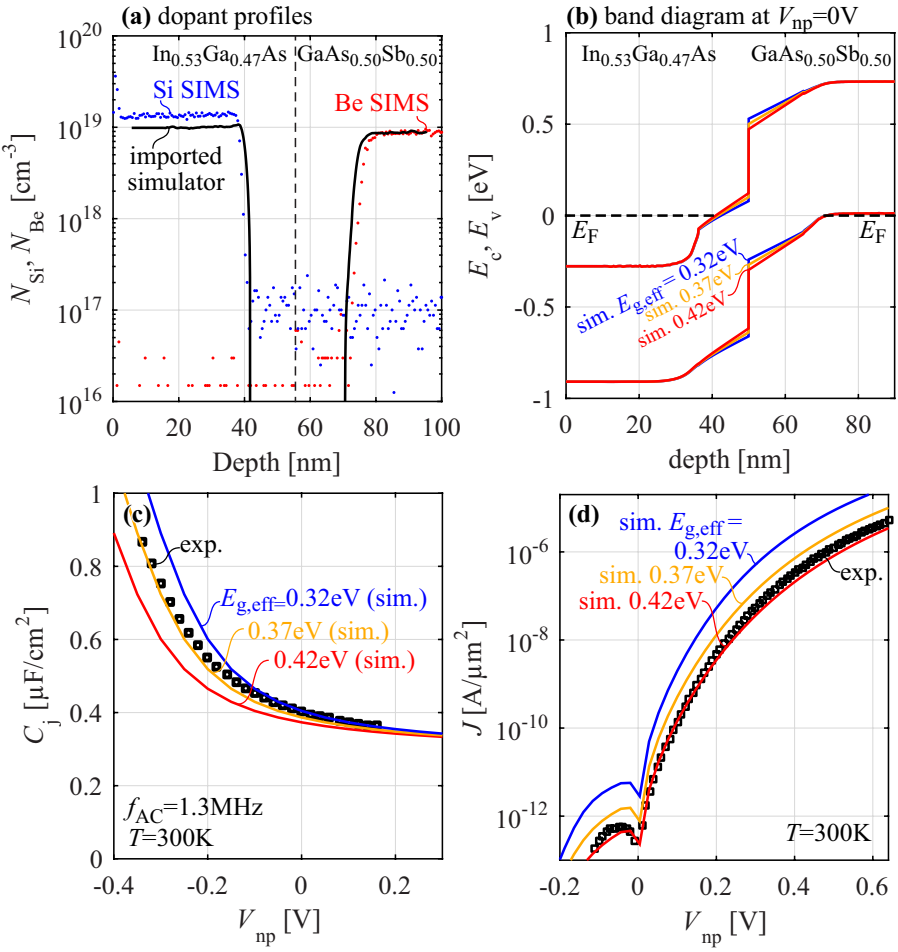


Figure 4.5: (a) The Beryllium and Silicon profiles are measured by SIMS (dots), and modified within the SIMS margins of error (full line) to obtain good agreement between simulated and measured (c) C-V and (d) I-V. (b) The band diagrams show $E_{g,eff}$ impacts the built-in electric field and tunnel path length at the heterojunction.

measurements are performed with a *Keysight E4980A* precision LCR meter. We correct for the parasitic capacitance of the contact pads, and we extract the junction capacitance shown in figure 4.5(c). The accuracy of these measurements is 0.7% (extracted in a similar way as section 3.4.4 on p.66), and the standard deviation on different devices is 1%, which is sufficiently low for our purpose.

The Silicon and Beryllium dopant profiles are measured by SIMS and are shown in figure 4.5(a). At the edge of the intrinsic region, the dopant slopes are steep, with a Silicon downslope of 1.4 nm/dec and a Beryllium upslope of 2.3 nm/dec. The location of the heterojunction is 55 nm (dashed line in figure 4.5(a)), determined from the SIMS intensity profiles of Indium and Arsenic.

4.2.6 Calibration of effective bandgap

In this section, we compare the experimentally extracted *I-V* and *C-V* traces with simulations, while taking $E_{g,eff}$ as a fitting parameter. We perform semi-classical simulations using Sentaurus Device from Synopsis [27], with the Jain-Roulston DOPBGN model introduced in section 2.2.4, with Fermi-Dirac statistics, with multivalley density of states model and nonparabolic correction [48, 64, 49] introduced in section 2.2.2. The bandgaps of undoped $In_{0.53}Ga_{0.47}As$ and $GaAs_{0.5}Sb_{0.5}$ are 0.74 eV [48] and 0.77 eV [35]. We set $E_{g,eff}$ by changing the electron affinity of $GaAs_{0.5}Sb_{0.5}$ only. The BTBT parameters of $In_{0.53}Ga_{0.47}As$ are A_{BTBT}=1.3 × 10^{20} cm^{-3} s^{-1} and B_{BTBT}=5.7 MV/cm, taken from the calibration in ref. [98]. These calibrated parameters are respectively 19% larger and 2% smaller than the values from Kane's theory [98]. For $GaAs_{0.5}Sb_{0.5}$, we calculate the parameters from Kane's theory, and we scale them up/down by the same 19% and 2%, and we obtain A_{BTBT}=1.7 × 10^{20} cm^{-3} s^{-1}, B_{BTBT}=6.3 MV/cm.

First, we import the SIMS dopant profiles directly in Sentaurus Device, and we compare the simulated and experimental *C-V* and *I-V* curves. We keep $E_{g,eff}$ as a fitting parameter, but we do not obtain a good match for any $E_{g,eff}$. We attribute this to inaccuracies in the depth and concentration scales of the SIMS measurement (section 3.4.5 on p. 68). We therefore modify the dopant profiles by compressing the depth scale by 10% and reducing the Silicon concentration by 30% (full line in figure 4.5(a)). With these values, which are within the SIMS margins of error, we obtain a best match between simulated and measured *C-V* and *I-V* (figures 4.5(c-d)), using $E_{g,eff}$=0.37±0.05 eV.

For the median value $E_{g,eff}$=0.37 eV, the simulated capacitance is 4% lower than the measurement, while the simulated BTBT current is about a factor 2 higher than the measurement. The discrepancy possibly originates in inaccurate Fermi level positions, inaccurate DOPBGN parameters or additional reflections at the heterojunction which are not considered by the semi-classical simulator [69]. To account for these uncertainties, we place the error bars ±0.05 eV on the calibrated $E_{g,eff}$=0.37 eV such that the simulations encompass the measured *C-V* and *I-V*.

4.2.7 Discussion

Our result ($E_{g,eff}$=0.37±0.05 eV) is in agreement with ref. [100] ($E_{g,eff}$=0.35 eV), obtained from low-temperature photoluminescence measurements and temperature-dependent bandgap narrowing data [71, 103]. The source of $E_{g,eff}$ in ref. [99] is unknown to us. Our result does not agree with the value $E_{g,eff}$=0.29 eV (full line in fig. 4.1), which is calculated from the electron affinities [48] and bandgaps [64] of each separate material, obtained by optical measurements. We attribute the mismatch to the large sensitivity of the electron affinity measurements to the semiconductor-vacuum interface reconstruction, which induces an electric dipole at the interface. This dipole is much smaller for semiconductor-semiconductor interfaces or semiconductor-oxide interfaces [107]. Our value of $E_{g,eff}$ is extracted directly from a semiconductor-semiconductor heterojunction and is therefore more reliable for TFET predictions.

4.3 Calibrating the effective bandgap in p+/n++ hetero-diodes

In this section, we focus on p+/n++ $GaAs_{0.5}Sb_{0.5}/In_{0.53}Ga_{0.47}As$ Esaki diodes, where BTBT occurs in heavily doped regions. The impact of DOPBGN on the BTBT rate is not well known, therefore we extract $E_{g,eff}$ with a new, alternative method, which does not require the BTBT rates.

In general, the method requires a p+/n++ or p++/n+ Esaki diode (figure 4.6(a,c)) with a staggered (type II) or straddled (type I) band alignment. The most highest doped region should be highly degenerate and the lowest doped region is lowly degenerate or non-degenerate. Semiclassical [59] (figure 4.6(b,d)) and Quantum Mechanical (QM) simulations at cryogenic temperature show a nearly exponentially increasing BTBT current with with increasing forward bias (V_c<V_{np}<0), which is unusual for p+/n+ Esaki diodes. V_c is the voltage where BTBT no longer increases exponentially and can be recognized visually. We will theoretically show that $E_{g,eff}$ can be extracted from V_c without requiring knowledge of the bandgaps or tunneling rates.

4.3.1 Origin of nearly exponentially increasing current

In order to intuitively understand the origin of the exponentially increasing current, we theoretically derive the approximate I-V relation for p+/n++ diodes (figure 4.6(a)). A similar derivation can be made for p++/n+ diodes

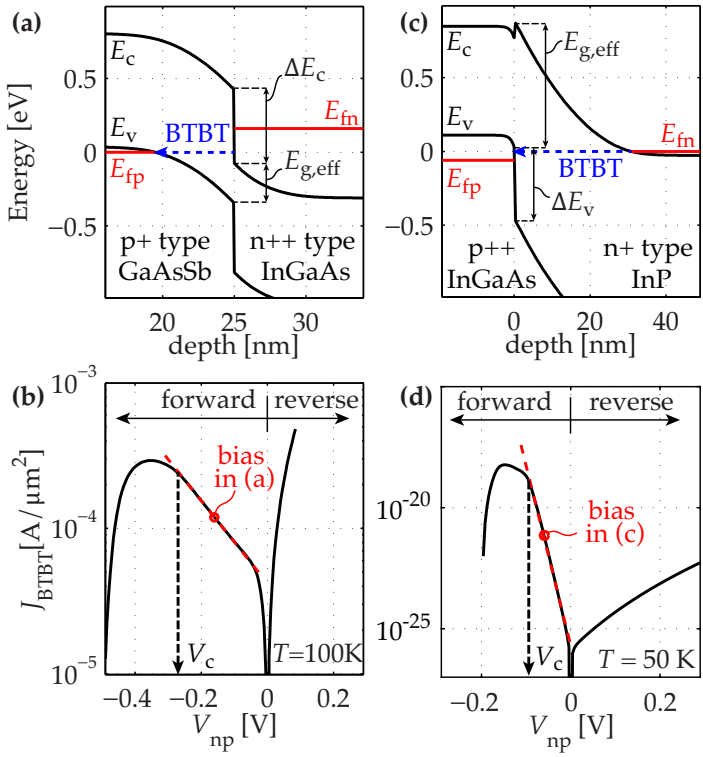


Figure 4.6: (a) The band diagram of a forward biased p+/n++ Esaki diode with staggered alignment shows tunneling from the heterointerface to the p+ region. E_c,E_v are conduction and valence band edges and E_{fn},E_{fp} are the quasi Fermi energy levels. (b) The corresponding simulation using Sentaurus Device [59] shows J_{BTBT} increases exponentially with forward bias at sufficiently low temperature. (c-d) show a similar behavior for a p++/n+ heterojunction with straddled alignment.

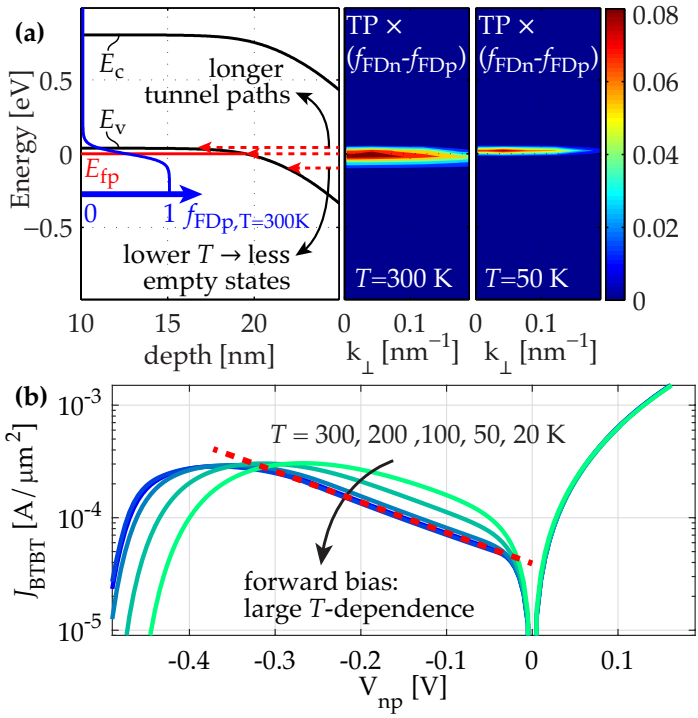


Figure 4.7: (a) The dashed arrows in the $GaAs_{0.5}Sb_{0.5}$ band diagram show suppressed tunneling at $E>E_{fp}$ and $E<E_{fp}$. The Transmission Probability (TP) weighted with Fermi-Dirac shows a peak in tunneling near E_{fp}, which is sharper for lower T. The TP is calculated with a 15-band k·p solver [62] and $k_\perp$ is the wavevector perpendicular to the tunneling direction. (b) Simulations [59] show that at small forward bias, J_{BTBT} is temperature dependent only for $T>100$ K.

(figure 4.6(c)). The exponential current originates from a sharp energy filtering mechanism. Tunneling occurs dominantly at $E=E_{fp}$, along a path which starts at the hetero-interface and ends in the p-type doped material (dashed arrow in figure 4.6(a)). Tunneling at the highest energy levels ($E>E_{fp}$) is suppressed because these tunnel paths are longer (figure 4.7(a)). At cryogenic temperature, tunneling at $E<E_{fp}$ is also suppressed due to a reduced amount of empty states $1\text{-}f_{FDp}(E)$, with $f_{FDp}(E)$ the Fermi-Dirac occupation in the p-type region. This causes a peak in tunneling near E_{fp}.

The BTBT current can therefore be described by considering tunneling only at $E{=}E_{\mathrm{fp}}$ and using the Wentzel-Kramer-Brillouin (WKB) approximation:

$$J_{\mathrm{BTBT}} \propto \exp\left(-2\int_0^{L_{\mathrm{t}}} \kappa\, dx\right) \tag{4.5}$$

where κ is the magnitude of the imaginary wavevector k along the tunnel path in the forbidden gap [29] and L_{t} is the length of the tunnel path.

Due to the quadratic band bending in $GaAs_{0.5}Sb_{0.5}$ (figure 4.8(a-b)), the shape of κ(x) in $GaAs_{0.5}Sb_{0.5}$ remains unchanged with more negative V_{np}, and only the limits of the integration change. For $V_{\mathrm{c}}{<}V_{\mathrm{np}}{<}0$, the value of $\kappa(x{=}0)$ is nearly constant because the tunnel path starts close to midgap. We can locally approximate that L_{t} decreases linearly with $-V_{\mathrm{np}}$ down to V_{c} (figure 4.8(f)). This causes J_{BTBT} to increase nearly exponentially (figure 4.8(e)). When $V_{\mathrm{np}}{<}V_{\mathrm{c}}$ the tunnel path extends into $In_{0.53}Ga_{0.47}As$ (figure 4.8(c-d)) and the current no longer increases exponentially, which allows the visual extraction of V_{c} from the I-V trace.

More rigorous simulations with a fully QM 15-band k·p solver [62] confirm the same trends in the I-V curve. Contrary to the WKB approximation, the QM simulations do not neglect wavefunction reflections due to the discontinuity in $\kappa(x)$ at the heterointerface [69, 68].

We can easily extract $E_{\mathrm{g,eff}}$ from V_{c}, because at this bias condition, E_{c} of $In_{0.53}Ga_{0.47}As$ at the hetero-interface is equal to E_{fp} (figure 4.8(b)). Therefore we obtain the relation

$$E_{\mathrm{g,eff}} = q(\Delta\Psi_{\mathrm{n}} + \Delta\Psi_{\mathrm{p}} - V_{\mathrm{c}}) - \xi_{\mathrm{n}} - \xi_{\mathrm{p}} \tag{4.6}$$

where q is the elementary charge, $\Delta\Psi_{\mathrm{n}}$, $\Delta\Psi_{\mathrm{p}}$ are the band bending of the n and p regions at $V_{\mathrm{np}}{=}V_{\mathrm{c}}$ (figure 4.8(b)) and ξ_{n}, ξ_{p} are the Fermi level degeneracies (shown in figure 4.8(d)) with

$$\xi_{\mathrm{n}} = E_{\mathrm{fn}} - E_{\mathrm{c,n,bulk}}$$

$$\xi_{\mathrm{p}} = E_{\mathrm{v,p,bulk}} - E_{\mathrm{fp}} \quad \text{(or zero if non-degenerate)}$$

In order to be valid for staggered and straddled heterojunctions, we define the effective bandgap at the hetero-interface as $E_{\mathrm{g,eff}}{=}E_{\mathrm{c,n}}{-}E_{\mathrm{v,p}}$ with $E_{\mathrm{c,n}}$ the n-type region conduction band edge and $E_{\mathrm{v,p}}$ the p-type region valence band edge, both taken at the hetero-interface (figure 4.6(a,c)).

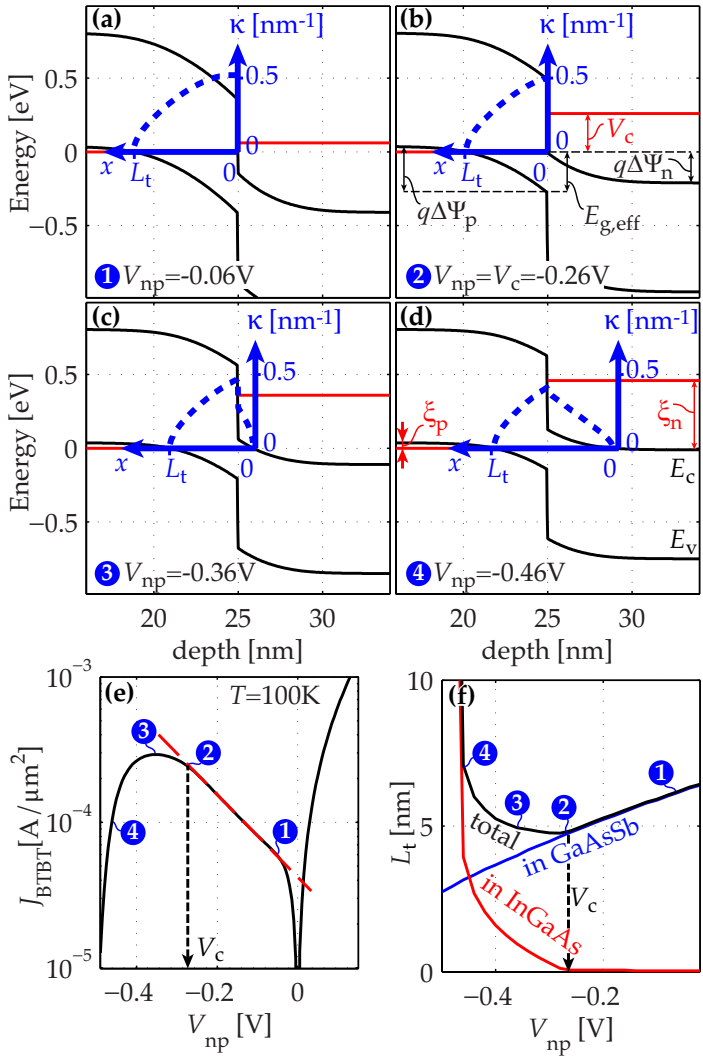


Figure 4.8: (a-d),(f) The tunnel path at $E{=}E_{\mathrm{fp}}$ is located entirely in $GaAs_{0.5}Sb_{0.5}$ for $V_c{<}V_{np}{<}0$, and extends to $In_{0.53}Ga_{0.47}As$ for $V_{np}{<}V_c$. κ is calculated using the Kane 2-band dispersion relation (introduced in figure 2.8(a) on p. 35). (e) The current no longer increases exponentially when $V_{np}{<}V_c$.

4.3.2 Requirements for nearly exponentially increasing current

We identify four requirements to obtain nearly exponentially increasing current in p+/n++ Esaki diodes. First, the temperature must be sufficiently low (figure 4.7(b)). Simulations show the required temperature decreases with higher p-type dopant concentration, lower $E_{g,\text{eff}}$ and higher degeneracy ξ_p. Experimentally this required temperature can be found easily by performing I-V measurements and lowering the temperature until the I-V no longer changes.

Secondly, intermixing of both semiconductors near the heterointerface must be sufficiently low. Simulations show that the current is no longer exponential if the intermixing region is larger than 1 nm .

Thirdly, the degeneracy ξ_n must be larger than the band bending of the n++ region at V_{np}=0, which is $\Delta\Psi_n$ in figure 4.8(a). This is easily achieved in n++$In_{0.53}Ga_{0.47}As$ due to its low conduction band density of states, but not in n++Silicon.

Finally, the conduction band offset at the hetero-interface (ΔE_c in figure 4.6(a)) must be positive and sufficiently large ($q\Delta E_c > \xi_n - q\Delta\Psi_n$) such that the tunnel path starts at the heterointerface at V_{np}=0. This is the case for n++$In_{0.53}Ga_{0.47}As$/p+$GaAs_{0.5}Sb_{0.5}$ but not for n++$In_{0.53}Ga_{0.47}As$/p+InP. Furthermore, simulations show that the method remains valid in the limit of a near-broken bandgap heterojunction with $E_{g,\text{eff}}$=0 eV.

4.3.3 Experimental verification

We experimentally verify our prediction of exponential BTBT current in a forward biased diode. A 600 nm p-$GaAs_{0.5}Sb_{0.5}$/50 nm n+$In_{0.53}Ga_{0.47}As$ heterojunction is grown on a lattice matched InP substrate with Molecular Beam Epitaxy (MBE) as described in reference [106]. The active dopant concentrations p=$1.1 \times 10^{19}\,\text{cm}^{-3}$ and n=$3.3 \times 10^{19}\,\text{cm}^{-3}$ are obtained with Hall measurements and satisfy the requirements for exponential BTBT current listed in the previous section. High Resolution High Angle Annular Dark Field Scanning Transmission Electron Microscopy (HR-HAADF-STEM) analysis in figure 4.9 confirms a sharp hetero-interface with less than 1 nm of intermixing. The diode fabrication flow is identical as for the p+/i/i/n+ diodes in section 4.2.2 on p. 93.

We measure the diode I-V characteristics with an *Agilent 4156C* parameter analyzer. The diodes with junction areas A_j=0.01−2 µm^2 show NDR characteristics. Larger diodes are short-circuited due to a BCB recess issue, similar to the p+/i/i/n+ diodes in figure 4.4(d) on p. 95. Perimeter effects

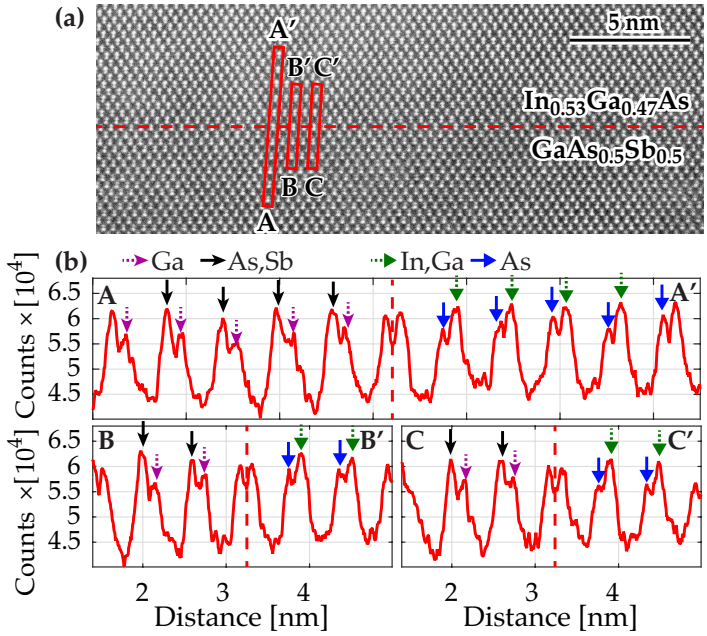


Figure 4.9: (a) HR-HAADF-STEM analysis and (b) the intensity traces along A-A', B-B' and C-C' show a locally smooth and sharply defined heterointerface with an intermixing region smaller than 1 nm and no visible defects.

are negligible, since I_{BTBT} scales with A_{j} in reverse (inset of figure 4.10) and forward bias.

We correct for series resistance R_{s} by considering the diffusion current in high forward bias (described in section 3.3.1 on p. 57). The measured V_{c} can be severely impacted by a high R_{s} if the I-V curves are not corrected. The peak voltage of diodes with A_{j}=0.04 µm^2 shifts by only 0.02 V, but diodes with A_{j}=2 µm^2 have a higher total current and the peak voltage is shifted by 0.1 V due to R_{s}=350 Ω.

When the temperature is lowered we observe a decrease of BTBT in forward bias, and the I-V becomes more exponential (figure 4.10) as predicted by simulations (figure 4.7(b)). The exponential current also confirms that the intermixing region at the heterojunction is smaller than 1 nm. At T=78 K we extract V_{c}=−0.27 V from 2 diodes with different areas.

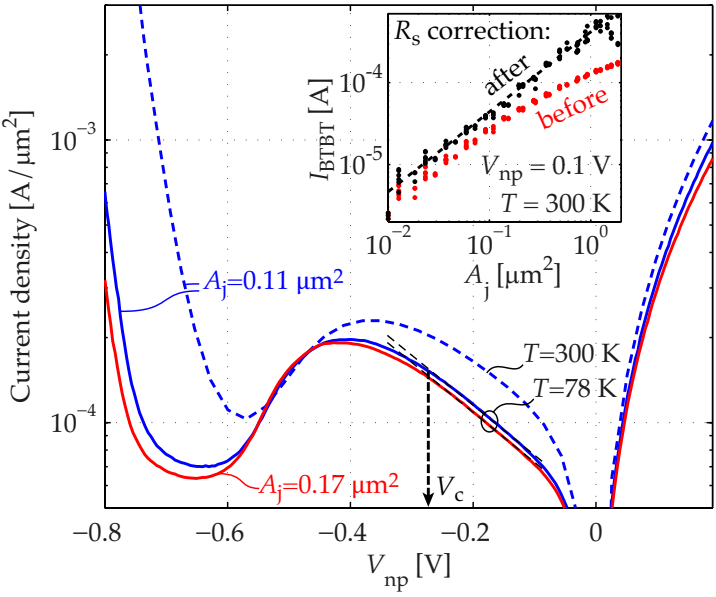


Figure 4.10: The measured I-V curves become more exponential at T=78 K. We extract V_c=−0.27 V from 2 diodes with different areas. The inset shows I_{BTBT} scales with the junction area, but only after correcting for series resistance.

4.3.4 Extraction of heterojunction effective bandgap

In order to extract $E_{g,eff}$ from V_c using equation (4.6), we calculate the degeneracies $\xi_{n,p}$ and band bending $\Delta\Psi_{n,p}$ at V_c using the measured active dopant concentrations and Sentaurus Device [59]. We use Fermi-Dirac statistics and the effective mass approximation for the light hole, heavy hole and conduction bands with a nonparabolicity correction in the Γ, L and X valleys [48, 64, 49]. We assume Dopant-dependent Bandgap Narrowing (DOPBGN) does not increase the degeneracy, and we obtain ξ_n=0.47 eV and ξ_p=0.04 eV at T=78K. We obtain a match between simulated and measured V_c=−0.27 V at T=78 K with $E_{g,eff}$=0.27 eV. We then extrapolate this result to T=300 K using literature data on temperature dependent bandgap narrowing [71, 103] and obtain $E_{g,eff}$=0.21 eV. Currently we cannot quantitatively compare the full measured and simulated I-V, as we do in section 4.2 for p+/i/i/n+ diodes, because this requires a profound understanding of the impact of DOPBGN on BTBT rates.

4.3.5 Sensitivity analysis

We assess the sensitivity of $E_{g,eff}$ to the different input parameters in equation (4.6) using semiclassical simulations. If an error $\Delta V_c = \pm 20\,mV$ is made during the experimental extraction in figure 4.10, this results in an error $\Delta E_{g,eff} = \pm 45\,meV$. If an error is made on ξ_n, ξ_p due to a possibly inaccurate density of states model, $\Delta\xi_p = \pm 20\,meV$ results in an error $\Delta E_{g,eff} = \mp 20\,meV$, and $\Delta\xi_n = \pm 20\,meV$ results in $\Delta E_{g,eff} = \pm 11\,meV$.

4.3.6 Discussion

Using these p+/n++ $GaAs_{0.5}Sb_{0.5}/In_{0.53}Ga_{0.47}As$ diodes, we have obtained $E_{g,eff} = 0.21\,eV$. This value is significantly lower than our result $E_{g,eff} = 0.37 \pm 0.05\,eV$ for p+/i/i/n+ hetero-diodes, even when considering the possible errors bars from section 4.3.5, .

We identify three possible explanations for this discrepancy. First, in the case of p+/i/i/n+ diodes, BTBT occurs in the nearly intrinsic regions. Similarly, the values listed in references [48, 19] are obtained from undoped materials. References [99, 35] list no source for $E_{g,eff}$. However, in the case of p+/n++ hetero-diodes, BTBT occurs in the highly doped regions which are strongly affected by DOPBGN. This could increase ξ_n and ξ_p and therefore also $\Delta\Psi_{n,p}$. This would result in a underestimated $E_{g,eff}$ for the same measured $V_c = -0.27\,V$. Our obtained value $E_{g,eff} = 0.21\,eV$ is therefore a lower limit.

The second possibility is a fixed interface charge affecting the band bending, as reported in reference [104] for a $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ heterojunction. It was reported that a fixed positive charge of $6 \times 10^{12}\,cm^{-2}$ changed the band alignment from staggered to broken. However, HR-HAADF-STEM analysis shows no visible defects in our diodes (figure 4.9), thus we do not expect fixed charge to affect the measured $E_{g,eff}$. Furthermore, the p+/n++ and p+/i/i/n+ hetero-diodes were epitaxially grown with nearly the same MBE recipe. It is unlikely that the p+/n++ stack would contain a fixed charge affecting the band bending, while the p+/i/i/n+ stack would be unaffected.

Thirdly, heavy doping could shift ΔE_c and ΔE_v and decrease $E_{g,eff}$, as suggested by Cho *et al.* [58]. We extrapolate $E_{g,eff} = 0.21\,eV$ to an undoped heterojunction using the literature values of Jain Roulston DOPBGN [58, 55] (introduced in section 2.2.4). This results in $E_{g,eff} = 0.39\,eV$, which agrees well with the value $E_{g,eff} = 0.37 \pm 0.05\,eV$, calibrated from p+/i/i/n+ diodes in section 4.2. As a guide to $GaAs_{0.5}Sb_{0.5}/In_{0.53}Ga_{0.47}As$ TFET designers, we plot the expected $E_{g,eff}$ as function of doping concentration in figure 4.11 for three

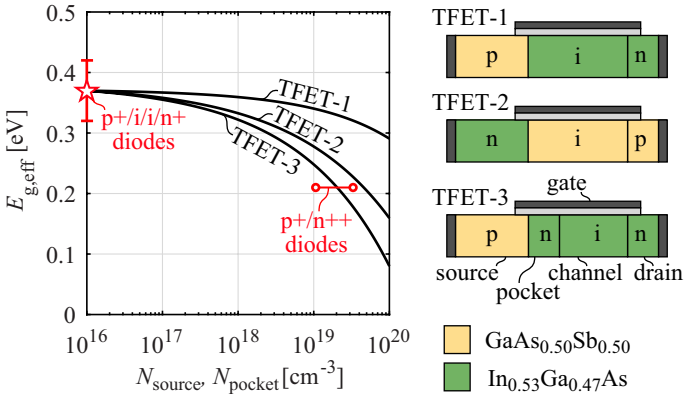


Figure 4.11: Expected impact of DOPBGN on $E_{g,eff}$ in three heterojunction TFETs with doped sources (and doped pocket for TFET-3). All traces are calculated with the Jain-Roulston DOPBGN model [58, 55]. The two circles indicate N_A=1.1 × 10^{19} cm^{-3},N_D=3.3 × 10^{19} cm^{-3}

different TFET configurations. TFET-1 has a p+GaAs$_{0.5}$Sb$_{0.5}$ source and an undoped In$_{0.53}$Ga$_{0.47}$As channel. The impact of doping on $E_{g,eff}$ is higher for TFET-2, which is an n-type TFET with a n+In$_{0.53}$Ga$_{0.47}$As source and an undoped GaAs$_{0.5}$Sb$_{0.5}$ channel. The impact is highest for TFET-3, which has a p+GaAs$_{0.5}$Sb$_{0.5}$ source, a counterdoped n+In$_{0.53}$Ga$_{0.47}$As pocket, and an undoped In$_{0.53}$Ga$_{0.47}$As channel.

4.4 Conclusions and future work

In conclusion, we have calibrated $E_{g,eff}$ in a lowly doped GaAs$_{0.5}$Sb$_{0.5}$/ In$_{0.53}$Ga$_{0.47}$As heterojunction and obtained $E_{g,eff}$=0.37±0.05 eV. We achieved this by comparing the simulated and measured I-V and C-V characteristics of p+/i/i/n+ hetero-diodes, using the calibrated BTBT parameters from chapter 3, and taking $E_{g,eff}$ as a fitting parameter. Our result is obtained directly from the tunneling current in this heterojunction, and is hence more reliable for TFET predictions than $E_{g,eff}$ values obtained from bandgaps and electron affinities which are sensitive to interface reconstruction.

The calibration was performed using experimental 'pure BTBT' characteristics, measured at T=77 K to suppress TAT, and extrapolated back to T=300 K. This extrapolation is achieved by modeling the temperature dependence of BTBT using $I_{BTBT} \propto \exp(c\,T^{3/2})$, derived from Kane's theory. We obtain much better

agreement with this model than with the activation energy model, where I_{BTBT} is modeled as an Arrhenius process with $I_{\mathrm{BTBT}} \propto \exp(-E_{\mathrm{A}}/(k_{\mathrm{B}}T))$, which does not have a physical origin. We recommend our model to other TFET researchers who wish to identify BTBT and extrapolate it to other temperatures.

In a second set of simulations and experiments, we have determined $E_{\mathrm{g,eff}}$ in a highly doped p+/n++ $GaAs_{0.5}Sb_{0.5}/In_{0.53}Ga_{0.47}As$ Esaki diode and obtained a lower limit $E_{\mathrm{g,eff}}$>0.21 eV. This value is consistent with $E_{\mathrm{g,eff}}$=0.37±0.05 eV obtained with p+/i/i/n+ diode, when we consider DOPBGN reducing $E_{\mathrm{g,eff}}$. We have achieved this result using a new method, exploiting an unusual feature of p+/n++ Esaki diodes, which is exponentially increasing BTBT current with forward bias at cryogenic temperature. The method only requires knowledge of the dopant concentrations and degeneracies $\xi_{\mathrm{n,p}}$ but does not require the bandgaps and tunneling rates. We have defined requirements to apply our method to other heterojunctions. The exponential current also allows us to determine that the intermixing region at the junction is <1 nm, which is verified by HR-HAADF-STEM analysis. Other applications include the analysis of fixed charge at the heterojunction and further understanding of DOPBGN and its impact on TFET.

For future work, we suggest performing Internal Photoemission (IPE) Spectroscopy to characterize the band alignment of the $GaAs_{0.5}Sb_{0.5}/In_{0.53}Ga_{0.47}As$ heterojunction, similar to the work of Nguyen *et al.* [108, 109]. With IPE, a semi-transparant gate stack is deposited on the III-V heterojunction, and monochromatic light is injected through the gate stack in the semiconductor. An electric field is applied by contacting the gate stack, and electrons and holes are excited over the oxide conduction and valence bands if the injected photon energy is sufficiently high. The onset of the photocurrent is measured at different electric fields, from which the band alignment is extracted. This method provides an alternative path to verify the hypothesis of DOPBGN lowering $E_{\mathrm{g,eff}}$. However, it is a less direct method, because the impact of DOPBGN is measured optically instead of using the BTBT current.

The results on the highly doped p+/n++ $GaAs_{0.5}Sb_{0.5}/In_{0.53}Ga_{0.47}As$ heterojunction have been presented at the Device Research Conference 2015 [110], and published in Applied Physics Letters in 2015 [111].

Chapter 5

Delayed BTBT onset due to field-induced quantum confinement

In chapter 3, we have calibrated BTBT models using homojunction tunnel diodes. In those devices the electrostatic potential ideally varies in only one dimension, which is also the tunneling direction. In a TFET however, the electrostatic potential varies in two or three dimensions due to the presence of the gate stack. In the direction of tunneling, which is at least partially oriented towards the gate stack, a triangular-like potential well is formed, causing Field-Induced Quantum Confinement (FIQC) of charge carriers [65]. In the particular case of the line-TFET configuration, the tunneling direction (dashed arrows in figure 5.1(a)) is fully perpendicular to the gate. The large and uniform electric field in the direction of tunneling allows steeper SS than with a point-TFET, but also leads to increased FIQC. It has been predicted, without experimental verification, that FIQC mainly causes a delayed onset of BTBT [65].

In this chapter, we experimentally demonstrate this delay of BTBT. We accomplish this by developing a method where the tunneling in a line-TFET is mimicked using a highly doped MOS capacitor, which we call the BTBT MOS-CAP. We discuss the operation principle of the BTBT MOS-CAP in section 5.1. We then discuss previous work about BTBT MOS-CAPs in literature in section 5.2, and we elaborate on our own FIQC measurement strategy in section 5.3. Using simulations, we predict the minimum required dopant concentration to obtain BTBT in MOS-CAPs in section 5.4

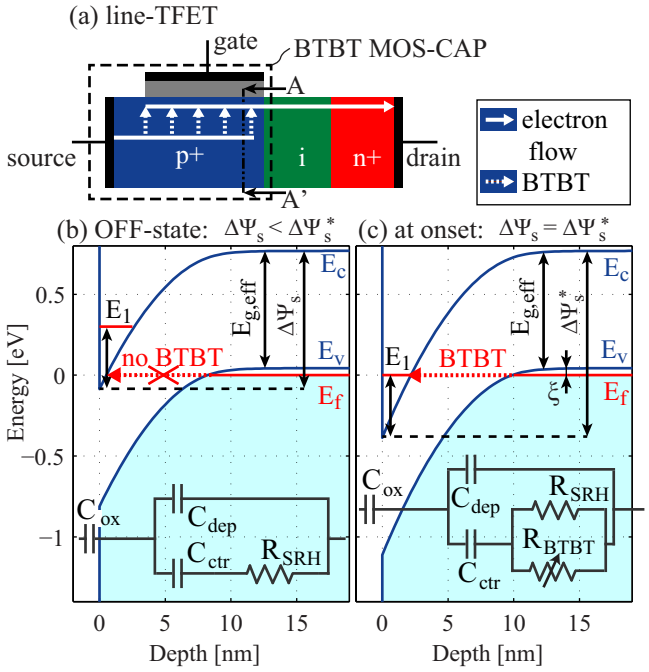


Figure 5.1: (a) The line-TFET and the BTBT MOS-CAP, of which the band diagrams along the cut line A-A' are shown (b) in off-state and (c) at BTBT onset. $E_{\mathrm{g,eff}}$ is the effective bandgap of the semiconductor, including temperature and dopant dependent bandgap effects. E_1 is the first subband energy. The shaded areas depict occupied states. $\Delta\Psi_\mathrm{s}$ is the semiconductor band bending, which reaches $\Delta\Psi_\mathrm{s}^*$ at BTBT onset. The insets show the equivalent circuit of the BTBT MOS-CAP, modeled after refs. [112, 113] while neglecting the interface and oxide trap circuit elements. The capacitance over the semiconductor depletion region is C_dep. In inversion, C_ctr captures the electron charge centroid located $\approx 1-2\,\mathrm{nm}$ away from the oxide/semiconductor interface, due to the low $\mathrm{In_{0.53}Ga_{0.47}As}$ conduction band density of states [114].

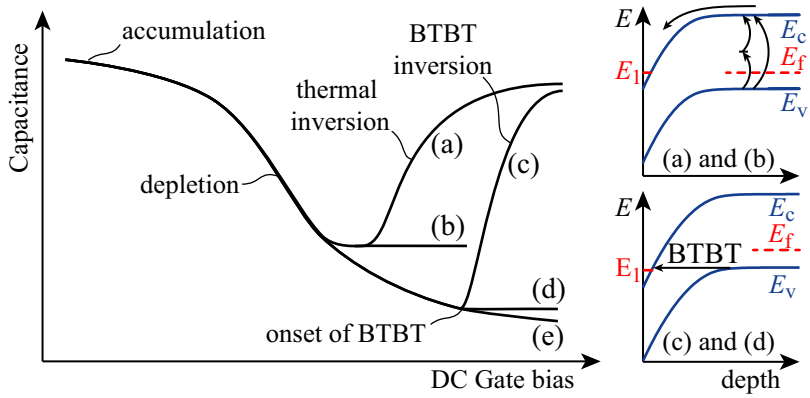
We discuss the fabrication of these MOS-CAPs in section 5.5. In section 5.6, we perform C-V measurements at cryogenic temperature to only allow minority carrier generation by BTBT and suppress the capacitive response of interface and border traps. With these measurements, we demonstrate AC inversion by BTBT which was so far unobserved in MOS-CAPs. In section 5.7, we then extract the semiconductor band bending at inversion onset from the C-V measurements, from which we calculate the first quantized energy level in section 5.8. We compare the experimentally obtained BTBT onset values with quantum mechanical predictions, and we obtain good agreement. We perform an uncertainty analysis of the extracted FIQC in section 5.9. Finally, in section 5.10 we propose the use of BTBT MOS-CAPs for BTBT calibration, and for characterization of traps deep into the conduction band.

5.1 BTBT MOS-CAP operation principle

In order to demonstrate FIQC while avoiding the complicated TFET fabrication and analysis, we introduce the use of a highly doped MOS-CAP, which is the key part of the line-TFET, as shown in figure 5.1(a). It consists of the highly doped source, the gate stack to apply band bending in the source, and the source contact. We call this device the BTBT MOS-CAP, because generation of the inversion charge happens dominantly by BTBT due to strong band bending. The electrostatics, charge distribution, and quantized energy levels of the BTBT MOS-CAP and the line-TFET are identical in depletion (figure 5.1(b)) and at the onset of tunneling (figure 5.1(c)).

This onset of tunneling occurs when occupied states in the valence band energetically align with empty states in the conduction band, for the case of a p-type MOS-CAP. The lowest energy of empty states in the conduction band is the first subband energy level, E_1. We will therefore extract E_1 from a measurement of the amount of band bending at BTBT onset.

This BTBT onset corresponds to the onset of inversion in a C-V measurement, under the condition that BTBT is the dominant process for the generation of inversion charge, and this generation is sufficiently high. In other words, if we perform a C-V measurement and we apply a 30 mV AC signal, the characteristic time constant τ_{BTBT} to charge the inversion capacitance by BTBT must be much smaller than $\tau_{\mathrm{AC}}=1/(2\pi f_{\mathrm{AC}})$, τ_{AC} is the characteristic time constant of the AC signal, and f_{AC} is the AC frequency, typically 1 kHz−1 MHz. If $\tau_{\mathrm{BTBT}} \ll \tau_{\mathrm{AC}}$, the BTBT generation rate is sufficiently fast, and 'follows' the AC signal. The change in DC signal is typically much slower. We define τ_{DC} as the time required to sweep the DC voltage by 30 mV. For our measurement



	τ_{DC}	τ_{AC}	inversion mechanism
(a)	$\gg\tau_{th}$	$\gg\tau_{th}$	Thermal generation is high, follows DC and AC signals.
(b)	$\gg\tau_{th}$	$\ll\tau_{th}$	Thermal generation follows DC signal only.
(c)	$\ll\tau_{th}$ $\gg\tau_{BTBT}$	$\ll\tau_{th}$ $\gg\tau_{BTBT}$	Thermal generation is negligible. BTBT generation is fast, follows AC and DC signals.
(d)	$\ll\tau_{th}$ $\gg\tau_{BTBT}$	$\ll\tau_{th}$ $\ll\tau_{BTBT}$	BTBT generation follows the DC signal only.
(e)	$\ll\tau_{th}$ $\ll\tau_{BTBT}$	$\ll\tau_{th}$ $\ll\tau_{BTBT}$	No inversion. Thermal and BTBT generation cannot follow DC or AC signals.

Figure 5.2: 5 different p-MOS-CAP measurement conditions result in different C-V curves. This sketch is adapted from [115]. The sketched band diagrams show that for a non-degenerate Fermi level, the onset of thermal inversion occurs at smaller band bending than the onset of inversion by BTBT. For a degenerate Fermi level, we expect inversion by BTBT and thermal inversion to occur at nearly the same onset.

conditions, this is typically 0.2 s. If $\tau_{BTBT}\ll\tau_{DC}$, the BTBT generation rate also 'follows' the DC signal. If the BTBT rate follows both the DC and AC signals, and thermal generation of minority carriers is suppressed, the C-V trace is expected to be like the sketch in figure 5.2, mode (c). The onset of BTBT then coincides with the onset of inversion.

Modes (a) and (b) in figure 5.2 represent the most common C-V measurements. The DC bias is swept in several seconds, and f_{AC}=1 kHz for mode (a) and 1 MHz for mode (b). This results in thermal generation of inversion charge. For

measurement (a) at f_{AC}=1 kHz, the system is in thermal equilibrium, and the thermal generation of minority carriers follows both the DC and AC signals. τ_{th} is smaller than both τ_{DC} and τ_{AC}. τ_{th} is the time constant for thermal generation of inversion charge, which is shorter for higher measurement temperature, or when traps are present causing SRH generation/recombination.

In modes (c) and (d), thermal generation is suppressed by lowering the measurement temperature, or is made negligible with pulsed C-V measurements, such that τ_{DC},$\tau_{AC} \ll \tau_{th}$. In section 5.6, we will suppress thermal inversion by performing the C-V measurements at $T \leq 40$ K. We expect that the inversion charge is dominantly generated by BTBT, if the dopant concentration and therefore the electric field is sufficiently high. This corresponds to a sufficiently short τ_{BTBT} compared to τ_{DC} and τ_{AC}. In section 5.4, we will estimate τ_{BTBT} using simulations.

The upper sketched band diagram in figure 5.2 shows that for a non-degenerate Fermi level, the onset of thermal inversion occurs when the available conduction band states with lowest energy (E_1) align with the Fermi level. The lower sketched band diagram shows the onset of inversion by BTBT occurs when E_1 aligns with filled states in the valence band. Therefore, for a non-degenerate Fermi level, the onset of inversion by BTBT happens at a higher band bending than the onset of thermal inversion. For a degenerate Fermi level, we expect inversion by BTBT and thermal inversion to occur at nearly the same onset.

5.2 Previous work in literature

BTBT in highly doped Silicon MOS-CAPs was first demonstrated in 1967 by Goetzberger and Nicollian [115]. They performed pulsed C-V measurements on MOS-CAPs with different dopant concentrations. The pulse time of 10 ms was sufficiently small to suppress thermal minority carrier generation in inversion, which is typically τ_{th}=100 ms in Silicon. For dopant concentrations $>1 \times 10^{18}$ cm^{-3}, they observed the semiconductor band bending would not increase beyond the bandgap, due to minority carrier generation by BTBT.

This measurement condition is shown in figure 5.2, mode (d). On the onset of BTBT, the build-up of minority carriers at the oxide/semiconductor interface prevents further extension of the depletion region at high gate bias. However, these minority carriers do not contribute to the capacitance because f_{ac} is sufficiently large. This results in a constant capacitance with respect to gate bias. We will compare the results of Goetzberger and Nicollian to ours in section 5.8.

5.3 Measurement strategy

The work of Goetzberger and Nicollian was unknown to us at the time of the experiments, and we have conceived a different measurement approach, corresponding to mode (c) in figure 5.2. We perform C-V measurements at cryogenic temperature to suppress thermal generation of minority carriers, and only allow minority carrier generation by BTBT, which is nearly temperature-independent.

We choose the dopant concentration sufficiently high such that the BTBT minority carrier generation follows both the DC and AC signals. The minority carriers then contribute to the capacitance, which result in AC inversion by BTBT. The calculation of the required minimum dopant concentration to obtain $\tau_{BTBT} \ll \tau_{\mathrm{AC}}, \tau_{\mathrm{DC}}$ (mode (c) in figure 5.2) is discussed in section 5.4.

Although BTBT MOS-CAPs with both p-type and n-type doping are possible, we only consider p-type $In_{0.53}Ga_{0.47}As$ samples for two reasons. First, there is reduced charging and discharging of parasitic interface traps and border traps when the p+$In_{0.53}Ga_{0.47}As$ MOS-CAP is biased near the BTBT onset condition. The Fermi level is then located in the conduction band, which is expected to have a lower amount of interface traps than the valence band [116]. Performing the C-V measurements at cryogenic temperature helps in suppressing the capacitive response of interface and border traps, because tunneling to these traps is temperature-activated [117]. Secondly, a more accurate measurement of the quantization is possible with p-type MOS-CAPs, because quantization is stronger in the $In_{0.53}Ga_{0.47}As$ conduction band than in the valence band due to the lower density of states.

An overview of our FIQC measurement strategy is shown in figure 5.3. First, we perform C-V measurements at cryogenic temperature to only allow minority carrier generation by BTBT and suppress the capacitive response of interface and border traps. These measurements are discussed in section 5.6. The second step is to extract the semiconductor band bending at inversion onset ($\Delta\Psi_{\mathrm{s}}^{*}$) from the C-V measurements. $\Delta\Psi_{\mathrm{s}}^{*}$ is shown in figure 5.1(c). We can extract this value either from the applied gate bias at inversion onset, or from the measured capacitance at inversion onset. Both options are discussed in section 5.7. Finally, we calculate E_1 from $\Delta\Psi_{\mathrm{s}}^{*}$ using the band diagram in figure 5.1(c). This is discussed in section 5.8.

Hence, our strategy to measure the first subband energy E_1 is straightforward. It only requires cryogenic C-V measurements on MOS-CAPs with high dopant concentration, and a Hall measurement to determine this concentration. We do not need a complicated TFET fabrication or comparisons with simulations or input parameters other than $E_{\mathrm{g,eff}}$, ξ and the semiconductor dielectric constant.

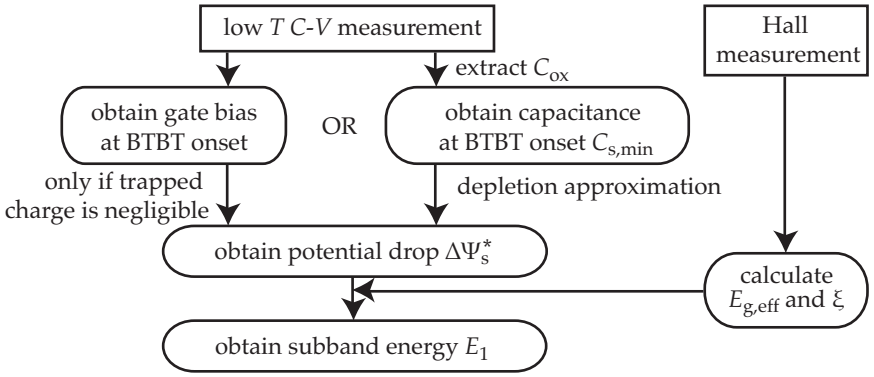


Figure 5.3: Overview of our FIQC measurement strategy.

5.4 Required dopant concentration for inversion by BTBT

In this section, we estimate which is the minimum dopant concentration required to have dominant inversion generation by BTBT in a $In_{0.53}Ga_{0.47}As$ MOS-CAP, biased just past the onset of tunneling. The BTBT generation must be sufficiently high to 'follow' the AC signal for the typical range $f_{AC} = 10^3 - 10^6$ Hz. This means the charge distribution and band bending must be independent of frequency for $f_{AC} < 10^6$ Hz.

In order to have dominant inversion by BTBT, we compare f_{AC} to time constant of BTBT τ_{BTBT}, obtained from the RC delay:

$$2\pi f_{AC} \ll \frac{1}{\tau_{BTBT}} = \frac{1}{R_{BTBT} C_{inv}}. \tag{5.1}$$

where R_{BTBT} is the resistance of the tunneling junction and C_{inv} is the inversion capacitance charged up by BTBT at each AC cycle. C_{inv} is the series connection of C_{ox} and C_{ctr}. C_{ox} is the oxide capacitance, and C_{ctr} represents the electron charge centroid located $\approx 1-2$ nm away from the oxide/semiconductor interface, due to the low $In_{0.53}Ga_{0.47}As$ conduction band density of states [114]. R_{BTBT}, C_{ox} and C_{ctr} are shown in the circuit diagram in the inset of figure 5.1(c) on p. 112.

To calculate R_{BTBT}, we start by considering three MOS-CAPs with p-type dopant concentrations $N_A = 2 \times 10^{19}$, 1×10^{18} and 5×10^{17} cm^{-3}. For different amounts of semiconductor band bending $\Delta\Psi_s$, we calculate the quantized energy levels in the conduction band with the 15 band k.p simulator, which is discussed

in section 2.2.6. We then determine the band bending $\Delta\Psi_s^*$ for which the lowest quantized energy level aligns with the highest occupied energy level in the valence band. In the low temperature limit, the latter is the Fermi level at the semiconductor contact, as shown in figure 5.1(c), or the valence band edge in case of non-degenerate doping.

Once this band bending $\Delta\Psi_s^*$ is obtained, we calculate the tunneling energy window, which requires the Fermi level efficiency of the gate stack. The Fermi level efficiency is defined as the change in semiconductor band bending for a given change in applied gate bias $\Delta\Psi_s/\Delta V_{gs}$ [118]. For a typical EOT=1.3 nm and N_A=2×10^{19} cm^{-3}, applying a 30 mV AC signal at the gate electrode results in a $\Delta\Psi_s$ change of only 21 mV, due to the potential loss over the oxide, and neglecting the impact of traps. Applying a 30 mV signal at the gate thus translates to a maximum tunneling energy window of 21 meV.

To obtain R_{BTBT}, we simulate the DC BTBT current per unit area in a line-TFET using Sentaurus Device. We apply a drain bias of V_{ds}=21 mV to match the tunneling window, and the gate bias V_{gs} is such that the same band bending is obtained in the line-TFET source as in the MOS-CAP. We then obtain R_{BTBT}=V_{ds}/J_{BTBT}. The resulting BTBT current densities are shown in figure 5.4. These semi-classical simulations are only an estimate, since they do not include the reduced density of states in the quantized region. However they do accurately capture the band bending and tunneling energy window. C_{inv} is calculated using the Modified Local Density Approximation (MLDA) model, which does account for the two dimensional Density of States (DOS) in the inversion layer and captures the centroid capacitance C_{ctr}.

The RC delay is calculated from equation 5.1 and shown in figure 5.4. For N_A=5×10^{17} cm^{-3}, τ_{BTBT}>1 ms and the tunneling current is too small to charge up the inversion layer for $f_{AC} = 10^3 - 10^6$ Hz. The MOS-CAP is then expected to be in depletion mode for all frequencies. When N_A>5×10^{18} cm^{-3}, the MOS-CAP is expected to be in AC inversion for all $f_{AC} = 10^3 - 10^6$ Hz (figure 5.4). When N_A=2×10^{19} cm^{-3}, the inversion layer is charged in only a few picoseconds.

5.5 BTBT MOS-CAP fabrication

Considering the simulation results from section 5.4, we choose four different p-type dopant concentrations (table 5.1). Reference samples 4a and 4b have the lowest concentration, for which we expect the BTBT generation rate to be very low. The capacitive response of minority carriers should be negligible for $f_{AC} = 10^3 - 10^6$ Hz. With the three other concentrations, we want to verify

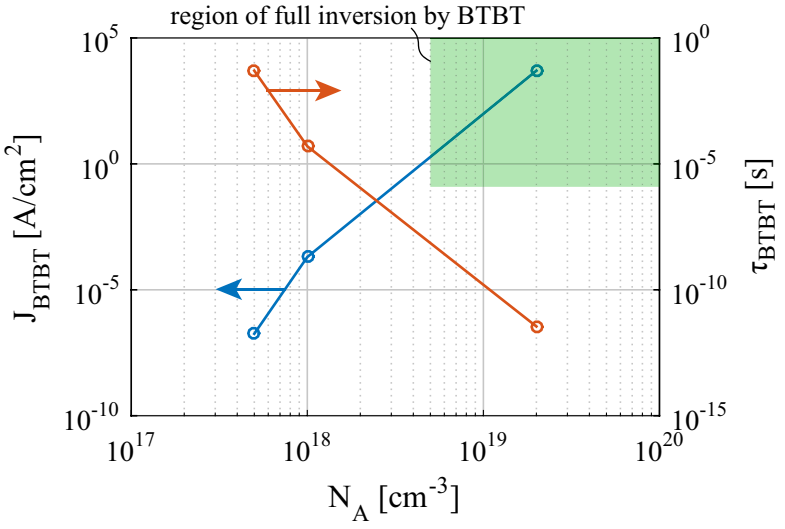


Figure 5.4: The maximum BTBT current density J_{BTBT} in MOS-CAPs, obtained from line-TFET simulations, increases rapidly for higher dopant concentrations. For $N_{\mathrm{A}}>5\times10^{18}\,\mathrm{cm}^{-3}$, the RC delay of tunneling τ_{BTBT} is much faster than the AC period at $f_{\mathrm{AC}}=10^3-10^6\,\mathrm{Hz}$. For these dopant concentrations and frequencies (green shaded region) we predict AC inversion by BTBT.

sample	1a	1b	2a	2b	3a	3b	4a	4b
$N_{\mathrm{A}}[\mathrm{cm}^{-3}]$	1.3×10^{19}		7.5×10^{18}		4.4×10^{18}		8.4×10^{17}	
t_{Al2O3} [nm]	2	8	2	8	2	8	2	8
C_{ox} [μF/cm^2]	2.0	0.76	2.2	0.75	2.0	0.74	2.2	0.75

Table 5.1: The samples are listed with their p-type dopant concentration (N_{A}) from Hall measurements, the target thickness of Al_2O_3, and the electrically extracted value of C_{ox}.

whether E_1 increases with higher dopant concentration due to the stronger electric field at onset.

These $In_{0.53}Ga_{0.47}As$ layers (600 nm thickness) are epitaxially grown by MBE on 2-inch InP (001) substrates (p-type doped $5\times10^{17}\,\mathrm{cm}^{-3}$) from AXT. The MBE growth is discussed in reference [116]. The native oxide is stripped with diluted HCl, and the surface is passivated with diluted ammonium sulfide.

The samples are then immediately transferred to an Atomic Layer Deposition (ALD) chamber for the deposition of Al_2O_3 (either 2 or 8 nm) and HfO_2 (2 nm). The different oxide thicknesses allow us to verify whether traps in the oxide and at the oxide/InGaAs interface have a parasitic contribution to the *C-V* measurement. A TiN gate is deposited and patterned using dry etching. Finally, the backside of the substrates is contacted using AuZn/Au and the samples are annealed in forming gas (H_2/N_2) for 5 min at T=370°C.

5.6 Cryogenic C-V measurements

The *C-V* characteristics are determined with a Agilent 4284A precision LRC meter. All *C-V* curves in the following figures are measured from inversion to accumulation, but in section 5.7 we discuss the impact of the inverse measurement (from accumulation to inversion). The equivalent parallel capacitance data of all samples is shown in figure 5.5. Sample 2b is measured at T=4 K. The other samples had contacting problems at T=4 K and the data at T=40 K is shown.

Inversion generation by BTBT in samples 1a, 2a, 3a and 1b, 2b, 3b is evident from the following three arguments. First, inversion is present at all measured temperatures (figure 5.6), since BTBT is not a thermally activated process. Secondly, inversion is observed only with the highest dopant concentrations (figure 5.5), as predicted in section 5.4. For those samples, inversion is present at all AC frequencies f_{AC}=1 kHz−0.5 MHz, since BTBT is very efficient at high electric fields. Finally, the inversion generation is not a perimeter effect, since the inversion capacitance scales with the MOS-CAP area (figure 5.7).

5.7 Obtaining the band bending at BTBT onset

We can extract $\Delta\Psi_s^*$ either through the value of the applied DC gate voltage at inversion onset, or through the value of the capacitance at onset. Which to use depends on the impact of trap charging in the oxide and at the oxide-semiconductor interface.

The first approach is also used in previous work by Goetzberger et al. on Silicon BTBT MOS-CAPs, which have a low trap density [115]. $\Delta\Psi_s^*$ is calculated from the applied DC gate voltage relative to the flat-band voltage. This calculation is straightforward when trapped charge is negligible, but complicated otherwise because an accurate trap density characterization is necessary. We first make the hypothesis that trapped charge is negligible, and calculate C_s-$\Delta\Psi_s$ curves from the *C-V* curves (figure 5.8). C_s is the semiconductor capacitance, and is equal

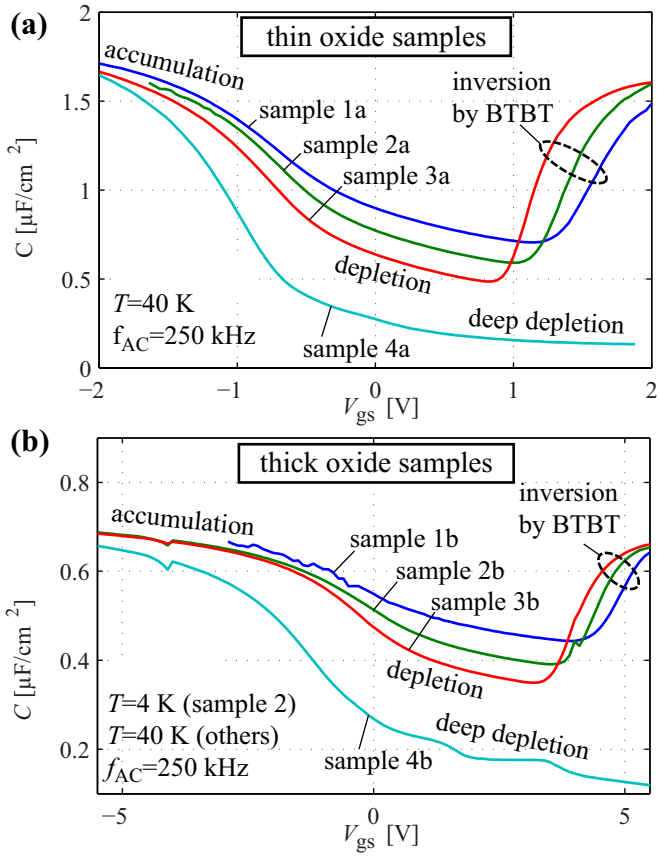


Figure 5.5: C-V measurements of samples with (a) thin and (b) thick oxides show inversion by BTBT when the dopant concentration is high. At high V_{gs}, gate leakage is high and the data is not shown. The fluctuations in capacitance at gate-source voltage V_{gs}=−4 V and 4 V are related to the measurement tool, and do not affect further interpretation of the results.

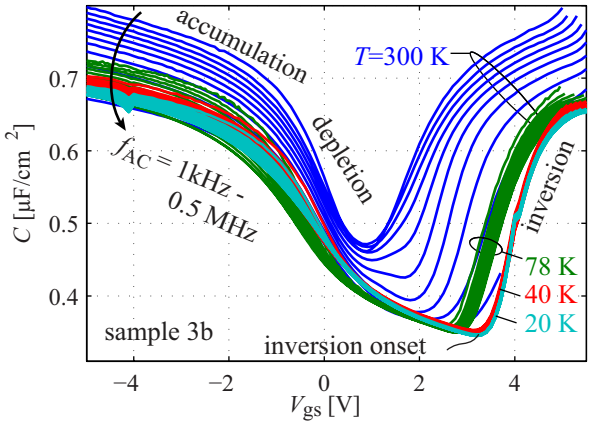


Figure 5.6: Inversion generation is present at all measured temperatures, since BTBT is not a thermally activated process. Below T=40 K there is very little frequency dispersion near inversion onset, indicating a suppressed oxide trap response. Vais *et al.* showed tunneling to oxide traps is a temperature-activated process [117].

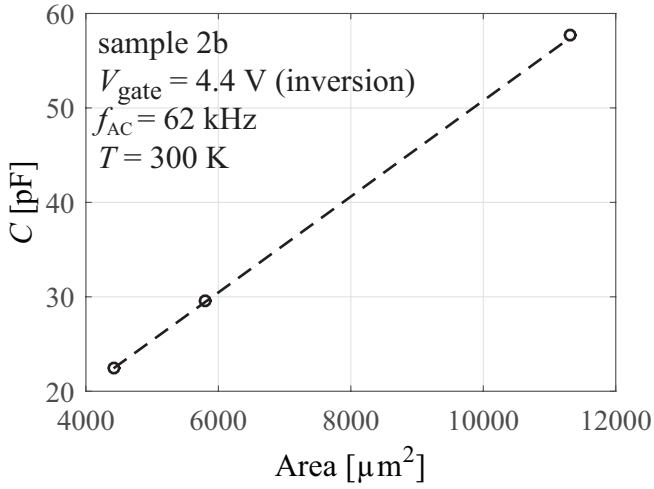


Figure 5.7: The inversion capacitance scales with the area. Therefore, the minority carrier generation at the MOS-CAP perimeter is negligible.

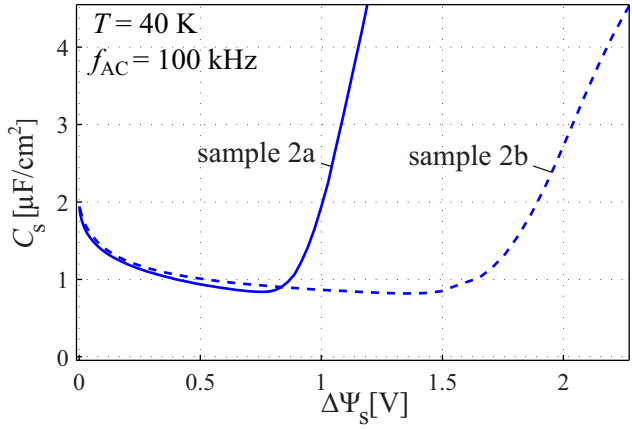


Figure 5.8: The C-V curves are converted to C_s-$\Delta\Psi_s$ curves, while assuming no trapped charge. This does not yield the same results for samples 2a and 2b, therefore charge trapping in the oxide is present. The flat-band condition $\Delta\Psi_s$=0 V is determined with the second derivative method [119].

to the depletion capacitance when the MOS-CAP is biased in depletion. C_s is extracted from the total measured capacitance by removing the contribution from C_{ox} (figure 5.9). The calculation is done for samples 2a and 2b, which have identical dopant concentration but a different oxide thickness. It should result in identical C_s-$\Delta\Psi_s$ curves if the hypothesis were correct, but the relative stretch-out between the two curves (figure 5.8) shows this is not the case, and thus we conclude that significant charge trapping occurs. Therefore, we cannot extract $\Delta\Psi_s^*$ using the applied DC gate voltage.

The second approach is to extract $\Delta\Psi_s^*$ from the value of the capacitance at onset. This value is not impacted by traps, as verified by the absence of frequency dispersion at cryogenic temperature (figure 5.6). We therefore can extract $\Delta\Psi_s^*$ by first removing the C_{ox} contribution from the measured complex impedance, then select the imaginary part to obtain the semiconductor capacitance C_s (figure 5.10). The onset of inversion is identified from the minimum of the latter, $C_{s,min}$, because at the corresponding value of V_{gs} the extrapolated linear semiconductor capacitance (in inversion) reaches zero. This V_{gs} is also the BTBT onset voltage of a line-TFET with identical semiconductor and gate stack.

In order to extract $\Delta\Psi_s^*$ from $C_{s,min}$ in a straightforward way, the depletion approximation is used: $\Delta\Psi_s^* = qN_A z_{d,max}^2/2\epsilon_s$ with the maximum depletion width $z_{d,max} = \epsilon_s/C_{s,min}$. The validity of the depletion approximation for our

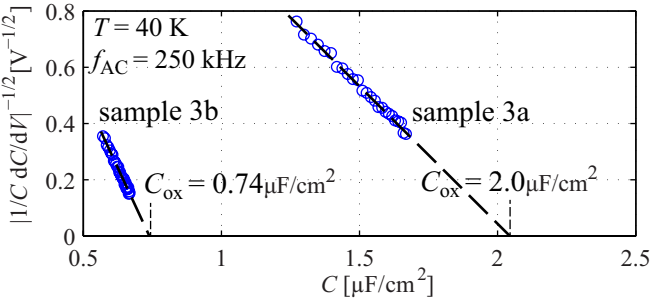


Figure 5.9: The values of C_{ox} listed in TABLE 5.1 are determined from extrapolation of the accumulation capacitance [120], and at T=40 K a good linear fit is obtained for all samples and frequencies, as shown here for samples 3a-b and f_{AC}=250 kHz. For sample 3a, we take the accumulation capacitance at $-2\,V<V_{gs}<-0.8\,V$. For sample 3b, we take $-4\,V<V_{gs}<-1\,V$

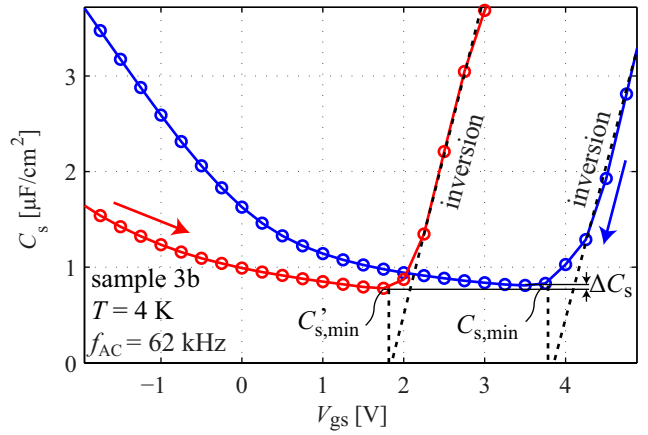


Figure 5.10: C_s at inversion onset $C_{s,min}$ is extracted by extrapolating the inversion capacitance to zero, coinciding with the point of minimum C_s. The hysteresis measurement shows there is a small uncertainty ΔC_s on $C_{s,min}$ due to the measurement direction (full arrows). This indicates the impact of interface charge on E_1.

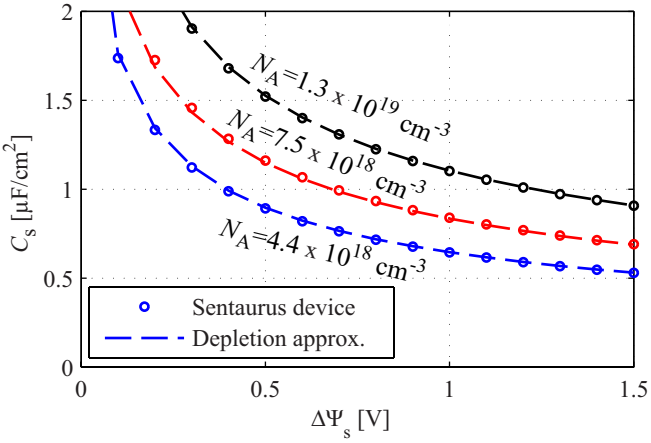


Figure 5.11: The accuracy of the depletion approximation is verified using Sentaurus device (with hole multivalley model), resulting in an error <0.5% at $\Delta\Psi_s$ near 1 V for the different dopant concentrations.

range of dopant concentrations and depletion widths is verified with Sentaurus Device (figure 5.11), and an error of less than 0.5% in C_s is obtained at $\Delta\Psi_s^*$, which is satisfactory for our purpose.

5.8 Quantized energy level extraction

E_1 is then calculated using $q\Delta\Psi_s^*=E_g+\xi+E_1$ (figure 5.1.c), where q is the electron charge and ξ is the degeneracy or 0 if non-degenerate. E_g and ξ are calculated based on the dopant concentration and measurement temperature, using Fermi-Dirac statistics (section 2.3.1) and dopant dependent band-gap narrowing (section 2.2.4). The experimentally obtained values of E_1 show increasing FIQC for higher dopant concentrations (circles in figure 5.12) due to the stronger electric field at onset.

We compare our experimentally extracted onset of BTBT with predictions from the Schrödinger solver based on a 15-band k·p model and hard wall boundary conditions (section 2.2.6), and good agreement is obtained (figure 5.12). We conclude that FIQC indeed causes a delayed onset of BTBT.

This FIQC observation is in agreement with previous C-V measurements on highly doped Silicon MOS-CAPs [121], where the inversion capacitance is

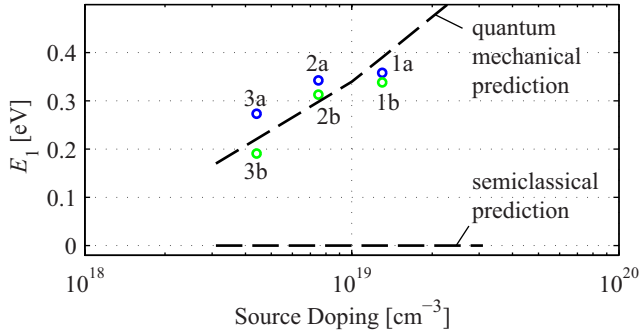


Figure 5.12: E_1 obtained by experiments (symbols) agrees well with 15 band k·p quantum mechanical simulations, but not with the semiclassical prediction of no FIQC.

generated thermally at T=300 K instead of by BTBT. However, our FIQC observation is not in agreement with the previous work by Nicollian and Goetzberger on Silicon BTBT MOS-CAPs [115], which showed a constant BTBT onset at $\Delta\Psi_s^*$=1.1 V which did not increase for higher dopant concentrations. We attribute this to the very thick SiO_2 layer ($50-100$ nm) which did not allow a sufficiently accurate measurement of $\Delta\Psi_s^*$.

5.9 Uncertainty and sensitivity analysis

There is an uncertainty on the obtained values of E_1 due to the sweep direction of V_{gs} during the measurement (figure 5.10). When sweeping from accumulation to inversion, the curves are shifted to more negative V_{gs}, indicating an increase of positive trapped charge (or decrease of negative trapped charge), and $C_{s,min}$ is slightly lower, resulting in about 25% uncertainty on E_1 due to the difference with measurement direction. Simulations indicate that an increase of positive charge (or decrease of negative charge) at the interface causes a less steep band bending in the semiconductor near the oxide interface, resulting in a higher first subband energy relative to the Fermi level. Therefore, a greater depletion width is required to reach BTBT onset.

We also assess the sensitivity of E_1 to the different input parameters, and calculate that 10% variation on N_A causes 30% variation on E_1. 10% variation on C_{ox} causes 20% to 40% variation on E_1, depending on the dopant level. The high sensitivity on extracted C_{ox} likely explains the systematically higher E_1 for samples 1-3a compared with samples 1-3b (figure 5.12). However, the total

uncertainty on E_1 remains small compared with the absolute values themselves, therefore not affecting the conclusion that FIQC causes a delayed onset of BTBT.

5.10 Potential applications for the BTBT MOS-CAP

5.10.1 Trap characterization

BTBT MOS-CAPs show promise for trap characterization. First, hysteresis measurements show that $C_{\mathrm{s,min}}$ is dependent on the sweep direction (figure 5.10) indicating that its value is a sensitive probe for the impact of interface traps on the semiconductor potential.

Secondly, at low temperature, the value of V_{gs} at BTBT onset provides a clear reference point for the E_{f}–V_{gs} relationship. The precise knowledge of the Fermi level position is a challenge in lowly doped MOS-CAPs, due to a trap-induced threshold voltage shift[112]. We propose performing simulations of the C-V characteristics that include trapped charge, and comparing these to measured C-V characteristics between the flat-band voltage and the onset of inversion. The trapped charge can be extracted from the stretch-out of the C-V curves.

Thirdly, we have shown that the Fermi level moves deep into the conduction band without Fermi level pinning. This allows the characterization of traps at this energy range. The response of the latter is shown by the frequency dispersion of the inversion capacitance at $T \geq 78\,\mathrm{K}$ (figure 5.6).

Finally, minority carrier generation by BTBT could allow the use of the full conductance method [112] using simple BTBT MOS-CAPs instead of more complicated MOSFETs. Martens *et al.* proposed the use of MOSFETs to provide an ample supply of minority carriers in the source and drain contacts. This allows characterizing traps near the conduction band edge, without the parasitic effect of a limited thermal generation of minority carriers. In highly doped BTBT MOS-CAP, the minority carriers are efficiently generated by BTBT, and the source/drain contacts are not necessary.

5.10.2 BTBT calibration

We propose performing BTBT calibration by using either high frequency AC measurements or pulsed measurements. In the first case, the applied f_{AC} is increased until the inversion charge can no longer be generated by BTBT sufficiently fast. This corresponds to measurement mode (d) in figure 5.2. For

this frequency, $f_{AC} = 1/(2\pi\tau_{BTBT})$, which allows the extraction of R_{BTBT} and calibration of a BTBT model by comparison with simulations. In the case of pulsed measurements, the pulse rise time is similarly shortened until the inversion capacitance no longer fully charges. This corresponds to measurement mode (e) in figure 5.2.

Similar to our calibration work in chapter 3, we can perform the calibration over a range of electric fields by measuring MOSCAPs with different dopant concentrations. From figure 5.4, we predict the pulse rise time should be a few microseconds in case of MOS-CAPs with a dopant concentration of N_A=$1 \times 10^{18}\,cm^{-3}$. If we increase N_A to $2 \times 10^{19}\,cm^{-3}$ which is a typical range for line-TFET, the measurements should be performed with either terahertz AC frequency or picosecond pulses, which is impossible with the current measurement technology. Therefore, this calibration should only be attempted on samples with a lower dopant concentration.

Compared to our calibration method using tunnel diodes in chapter 3, the method has the advantage of similarity between the BTBT MOS-CAP and the line-TFET. The effect of FIQC on the tunneling rate would be captured during the measurement.

5.11 Conclusion

The delayed onset of BTBT due to FIQC, predicted by quantum mechanical simulations, has been confirmed experimentally for the first time. Since FIQC occurs in nearly all TFETs, researchers should include it in all TFET simulations. The easy-to-fabricate BTBT MOS-CAP allows the measurement of the onset voltage of a line-TFET, and is promising for the characterization of traps deep into the conduction band.

The work in this chapter was presented at the Device Research Conference 2014 [122] and published in Applied Physics Letters [123].

Chapter 6

Cryogenic pulsed I-V measurements on III-V TFETs

In this chapter, we investigate whether we can suppress parasitic oxide trap charging and parasitic SRH/TAT generation in TFETs by performing pulsed I-V (PIV) measurements. The goal is to gain additional insight in these non-idealities, and to investigate whether trapping-free transfer characteristics can be achieved with cryogenic PIV measurements.

We start with a literature review of previous PIV measurements on MOSFETs and TFETs in section 6.1. We make a classification of effects of traps in section 6.2, and we define the goal of our measurements more precisely in section 6.3. We proceed with an overview three TFETs considered for these measurements, their C-V characteristics and their temperature-dependent DC I-V characteristics in sections 6.4-6.6. We elaborate on our pulsed I-V circuit configuration in section 6.7, the single pulse and multi pulse methods in section 6.8, and possible pitfalls in section 6.9. Both PIV methods are verified using a nearly trap free Silicon MOSFET in section 6.10, and we perform PIV measurements on the three TFET in section 6.11 and we discuss the results in section 6.12.

All measurements in this chapter were performed at the Physical Measurement Laboratory at the National Institute for Standards and Technology (NIST) in Maryland, USA, in a collaboration between imec, NIST and Penn. State University.

6.1 Pulsed I-V literature review and introduction

Pulsed *I-V* (PIV) characterization was performed for the first time by Kerber *et al.* from imec [124]. The purpose was to characterize fast transients in the drain-source current (I_{ds}) of Silicon MOSFETs with a defect-rich high-k gate oxide. The PIV method consists of biasing the MOSFET in an initial 'de-trapping' bias condition. Then, the gate-source voltage (V_{gs}) is rapidly swept using a pulse generator, while I_{ds} is measured with an oscilloscope. When V_{gs} is swept much faster than the response time of the oxide traps, which is typically on the order of microseconds [125], a more ideal I_{ds}-V_{gs} trace is observed, compared to a 'slow' and degraded Direct Current (DC) measurement performed in several seconds.

The reason for the degraded DC measurement can be understood as follows. When V_{gs} of and n-type MOSFET is increased, the oxide and Silicon channel energy bands bend down. Defect states in the oxide are then gradually filled up with electrons, or they gradually release positive charges, as their energy reaches the Fermi level. This increase in negative charge reduces the rate of band bending in the semiconductor and causes a stretch-out of the I_{ds}-V_{gs} characteristics, or a threshold voltage (V_t) shift. If the density of defects is very high, this causes Fermi level pinning.

The main application of the PIV method is to perform the I_{ds}-V_{gs} sweeps in both shorter and longer times than the time constant of traps τ_t. This allows characterizing slow vs fast trapping, positive vs negative trapped charge, and bias temperature instability [124, 126, 127, 125]. A second application is to completely suppress charging of traps and reveal the 'intrinsic' MOSFET performance.

In 2010, Young *et al.* [125] performed PIV measurements at a range of different speeds on Silicon MOSFET with a SiO_2/HfO_2 gate oxide. Young observed improving I_{ds}-V_{gs} characteristics when decreasing the measurement time from 4 s to 5 µs, but no further improvement from 5 µs to 40 ns. Young concluded that trapping-free characteristics are obtained when measuring faster than 5 µs. At those speeds, charging of traps in the HfO_2 layer is prevented by the high-quality 1 nm SiO_2 interfacial layer, which physically separates the traps from the channel electrons.

However, compared to MOSFETs, TFETs often have dominant trap-related Shockley-Read-Hall (SRH) and Trap-Assisted-Tunneling (TAT) leakage mechanisms in the off-state. Therefore, researchers investigated whether SRH and TAT could by suppressed by performing PIV measurements. In 2012, Mohata *et al.* performed PIV measurements on TFETs for the first time [128], to benchmark the trap-free device performance. The studied device was a nanopillar-based

$In_{0.53}Ga_{0.47}As$ TFET with a Al_2O_3/HfO_2 ALD gate oxide on the sidewall. Pulsed measurements decreased SS_{min} from 160 mV/dec to 100 mV/dec, attributed to suppressed interface traps. More recently, Rajamohanan *et al.* and Pandey *et al.* performed PIV measurements on InGaAs/GaAsSb TFETs with similar performance improvements [102, 129, 44, 18].

In 2013, Knoll *et al.* performed PIV measurements on Si nanowire TFETs by pulsing both the gate and the drain voltages simultaneously [130, 131]. Knoll observed a similar improvement of the swing in the transfer characteristics. We expect that the initial charge state of the defect is further modified by also pulsing the drain.

6.2 Classification of traps

We make the following classification in the effects of traps:

- Charge capture or emission by traps at the semiconductor/oxide interface or inside the oxide. This does not contribute to additional current but only leads to electric field screening and hence V_{gs} stretch-out.
- SRH and TAT generation (charge capture *and* emission) by traps at the semiconductor/oxide interface or inside the semiconductor, leading to increased I_{off}.

The previous references to MOSFET PIV measurements [124, 126, 127, 125] deal exclusively with the first effect. The references to TFET PIV measurements [128, 102, 129, 44, 18, 130, 131] deal with both effects simultaneously, because SRH and TAT are a more important problem for TFET. Contrary to Young's results for MOSFETs [125], increasingly faster TFET PIV measurements have always resulted in increasingly better performance.

We will now predict how PIV impacts the first effect, charging and discharging of oxide defects. We recommend modeling the impact of PIV on the second effect in future work. Charging and discharging of oxide defects has been described by inelastic tunneling [117]. Capture of a charge carrier in the semiconductor by an oxide trap at a distance x from the interface occurs with a characteristic trap time constant τ_t given by [132, 133, 118, 117]

$$\tau_t^{-1} = N_s v_{th} \sigma_0 \exp(-2\kappa x) \exp\left(-\frac{\Delta E_b}{k_b T}\right) \tag{6.1}$$

where N_s is the density of free carriers interacting with the trap and in the semiconductor, v_{th} is the thermal velocity, σ_0 is the trap cross-section, κ is the

imaginary part of the wavevector in the forbidden band, ΔE_b is the thermionic energy barrier height between the electron and trap states, k_b is the Boltzmann constant and T is the temperature [117]. Note that τ_t is independent of the trap density.

In a hypothetical experiment which mimics PIV, we consider a density of traps $N_\mathrm{t}(x)$ at depth x in the oxide and with an energy level E_t. The de-trapping condition is such that all oxide traps are empty at time t=0, and we monitor the time evolution of the trapped charge $Q_\mathrm{t}(x,t)$ at depth x [132]:

$$Q_\mathrm{t}(x,t) = -qN_\mathrm{t}(x)\left[1-\exp\left(-\frac{t}{\tau_\mathrm{t}(x)}\right)\right]\left[1+\exp\left(\frac{E_\mathrm{t}-E_\mathrm{F}}{k_\mathrm{b}T}\right)\right]^{-1} \quad (6.2)$$

where q is the electron charge, E_F is the Fermi level. The time evolution of $Q_\mathrm{t}(x,t)$ is determined by the negative exponential dependence. Therefore, if we perform PIV with a measurement time $t_\mathrm{meas} \ll \tau_\mathrm{t}$, the trapped charge will be lower than the equilibrium value, hence its negative impact on the I_ds-V_gs characteristics will be partly suppressed. In the limit $t_\mathrm{meas} \to 0$, its impact will be fully suppressed.

6.3 Goal of PIV measurements on TFET

The performance measured by PIV is important for TFET circuit simulations. A low-power TFET core would typically be operated at 500 MHz, which corresponds to a rise time and fall time t_r, t_f <1 ns. If the trapping time constant ≫1 ns, the traps have a smaller impact on the circuit performance during high-frequency operation. Therefore, more realistic circuit predictions can be achieved by considering the PIV characteristics and including the trapping time constants in the simulations.

In this chapter, we investigate which trapping mechanisms are suppressed by PIV: charge trapping by interface/oxide traps, and/or leakage by SRH and (thermally assisted) TAT. All these mechanisms can also be suppressed by decreasing the measurement temperature to T=4 K. The charge trapping mechanisms have a thermal activation step in equation (6.1), and the SRH/TAT generation are also strongly temperature dependent through the intrinsic carrier concentration $n_\mathrm{i}(T)$ in equation (3.8) on p. 76. A first goal is to verify whether we can obtain a similar improvement of the transfer characteristics by performing PIV measurement at room temperature.

By lowering the temperature near absolute zero, we expect that SRH and (thermally assisted) TAT generation can be fully suppressed. However, by performing PIV, we do not expect to suppress SRH/TAT to a lower current

than in the initial 'de-trapping' bias condition, right before the rising edge of the pulse. Instead, we presume the lowest measured SRH/TAT current depends on the initial charge state of the defects, and is therefore similar to the current in the 'de-trapping' bias condition.

A second goal is to attempt to reveal the 'intrinsic' TFET performance by slowing down charge trapping at T=77 K and T=4 K, and perform PIV at these temperatures. In future work, these trap-free characteristics can be compared to quantum mechanical simulations without TAT, SRH and interface traps and oxide charge trapping. This allows us to verify if we fully understand the BTBT component in TFETs, or achieve learnings about parasitic effects like band tails or a fixed charge at the hetero-junction.

To summarize, we will attempt to answer the following research questions in this chapter:

- By performing PIV, can we suppress charge trapping by defects inside the gate oxide and at the oxide/semiconductor interface? Can we suppress additional current generation by SRH and TAT, compared to the initial de-trapping bias condition? For which pulse times do we suppress these mechanisms?
- Can we sufficiently slow down the trapping mechanisms by lowering the temperature to T=4 K, and obtain fully trap-free transfer characteristics using PIV?

6.4 Studied TFETs

In this chapter we analyze the DC and PIV characteristics of three III-V nTFETs. Figure 6.1(a) shows a sketch of the first TFET, which we call the 'imec TFET'. It is a homojunction $In_{0.7}Ga_{0.3}As$ planar TFET, and it was presented by Alian *et al.* at IEDM in 2015 [21]. The source region is doped with Zinc, introduced by diffusion from a spin-on glass. It has been reported that this process induces a lower amount of dopant-related defects compared to in-situ doping, and therefore lowers TAT [17]. The electrical width of the imec TFET is W=400 µm, but all results are plotted in total current.

The other two TFETs were fabricated at Penn. State Univ. and therefore we call them 'PSA' and 'PSB'. Pandey *et al.* presented PSA at VLSI 2015 [18] and PSB at IEDM 2015 [134], and their colored TEM images are shown in figure 6.1(b-c). They are both vertical nano-pillar based $In_{0.65}Ga_{0.35}As/GaAs_{0.4}Sb_{0.6}$ TFETs. The main (targeted) difference between the two devices is the gate oxide, which

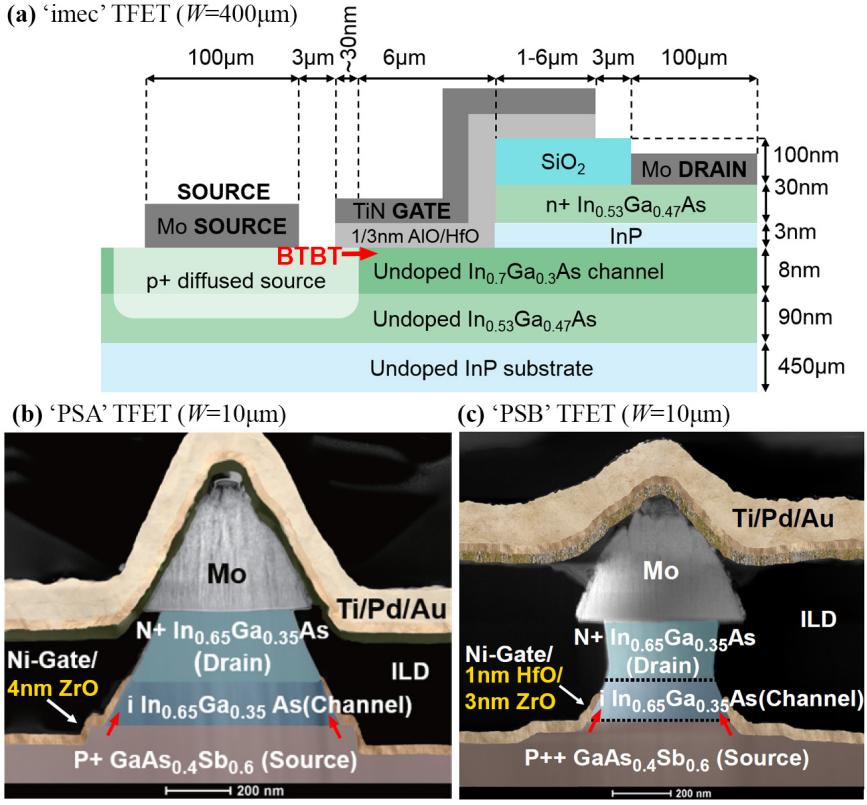


Figure 6.1: (a) The imec TFET has a planar homojunction design. (b-c) The colored TEM images show the PSA and PSB TFETs are staggered gap heterojunction TFETs with a vertical nano-pillar design. The images are adapted from references [18, 134]. The red arrows show where BTBT occurs, near the source/channel/oxide intersection.

is either 4 nm ZrO for the PSA TFET or 1 nm HfO_2/3 nm ZrO_2 for the PSB TFET. The electrical width is W=10 µm for both devices.

6.5 C-V characteristics

In this section, we perform C-V measurements on the imec and PSA TFETs. These will be used in section 6.9.3 to predict the RC delay and the resulting upper speed limit for the PIV measurements. We propose a simplified TFET equivalent circuit in figure 6.2(c), with separate gate-source (C_{gs}) and gate-drain (C_{gd}) capacitance contributions, at both sides of the tunneling junction. C_{gd} includes the gate-channel and gate-drain capacitance. The tunneling, source and drain resistances are R_t, R_s, and R_d.

The C-V characteristics are measured using a Keysight E4980A precision LCR meter and shown in figure 6.2(a-b). We perform measurements in either floating source or floating drain configuration, and we use the equivalent circuit of series C^*_{gd}-R_{eq} and C^*_{gs}-R_{eq}, as shown in figure 6.2(d-e). We place on asterisk symbol on the measured C^*_{gd} capacitance, because is not the true C_{gd}. In the floating source measurement, if the gate bias is low, R_t>1 MΩ and $C^*_{gd} \approx C_{gd}$. If the gate bias is high, R_t<200 Ω, C_{gs} also charges and $C^*_{gd} \approx C_{gs}+C_{gd}$. The same reasoning is valid for C^*_{gs}. Therefore, $C^*_{gd} \approx C^*_{gs}$ when the gate bias is high, which is confirmed in figures 6.2(a-b).

The imec device has $C_{gs}+C_{gd}$=60 pF in the on-state, which is quite high due to the micrometer size overlap dimensions. This places the upper limit on speed of the measurements, which will be calculated in section 6.9.3. For the PSA and PSB devices we measure a low $C_{gs}+C_{gd}$ ≈2 pF in the on-state because the overlap dimensions are much smaller. This will allow much faster PIV measurements.

6.6 DC characterization at 300, 77, 4K

We measure the DC transfer characteristics at T=300, 77, 4 K using a HP4156a precision parameter analyzer and a LakeShore CPX probe station. Figures 6.3(a,c,d) show a strong decrease in I_{off} with decreasing temperature, suggesting dominant SRH or TAT generation in the off-state. Figure 6.3(b) shows the calculation of new DC characteristics which include a 50 Ω series resistance at the source, for a fair comparison with PIV characteristics. The reason for the 50 Ω resistance will be discussed later in section 6.9.2.

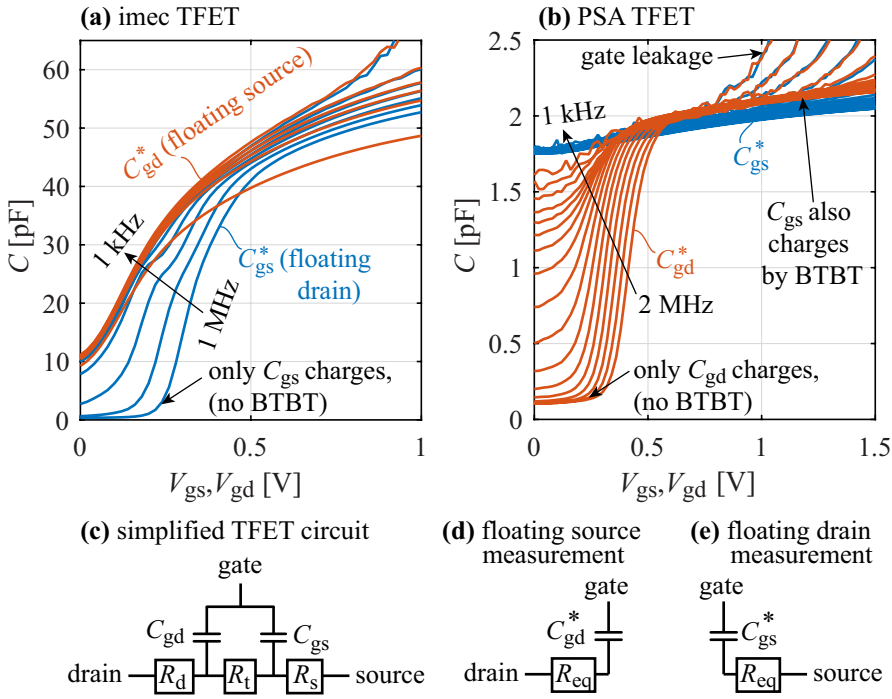


Figure 6.2: (a-b) C-V measurements are performed in (d) floating source or (e) floating drain configuration, to identify C_{gd} and C_{gs} and determine the upper PIV speed limit in section 6.9.3. (c) We propose an equivalent TFET circuit with separate gate-source (C_{gs}) and gate-drain (C_{gd}) capacitance contributions. The tunneling, source and drain resistances are R_t, R_s, and R_d.

For the imec TFET, more detailed temperature-dependent DC measurements in the range between 77 K and 400 K were performed by Alian *et al.*[21]. The extracted activation energy shows dominant SRH generation in the off-state, near V_{gs}=0 V, and increasing SRH current with increasing V_{gs}. This could be explained by our calibrated simulations of SRH in TFET in section 3.9.1 on p. 83, which agree qualitatively with the experimental results. It is possible that SRH is generated in the highly doped source region where the gate overlaps the source (an estimated 30 nm long, from the Zinc diffusion depth). However, the measured SRH current (I_{ds}=2 nA µm^{-1} at V_{gs}=0 V V_{ds}=0.5 V and T=300 K) is four orders of magnitude higher than the simulated bulk SRH current for the same bias condition (I_{ds}=10 − 100 fA µm^{-1}). Therefore, it is more likely that SRH is generated by defects at the semiconductor/oxide interface, instead of the bulk of the semiconductor. In any of the two cases, we expect that fast

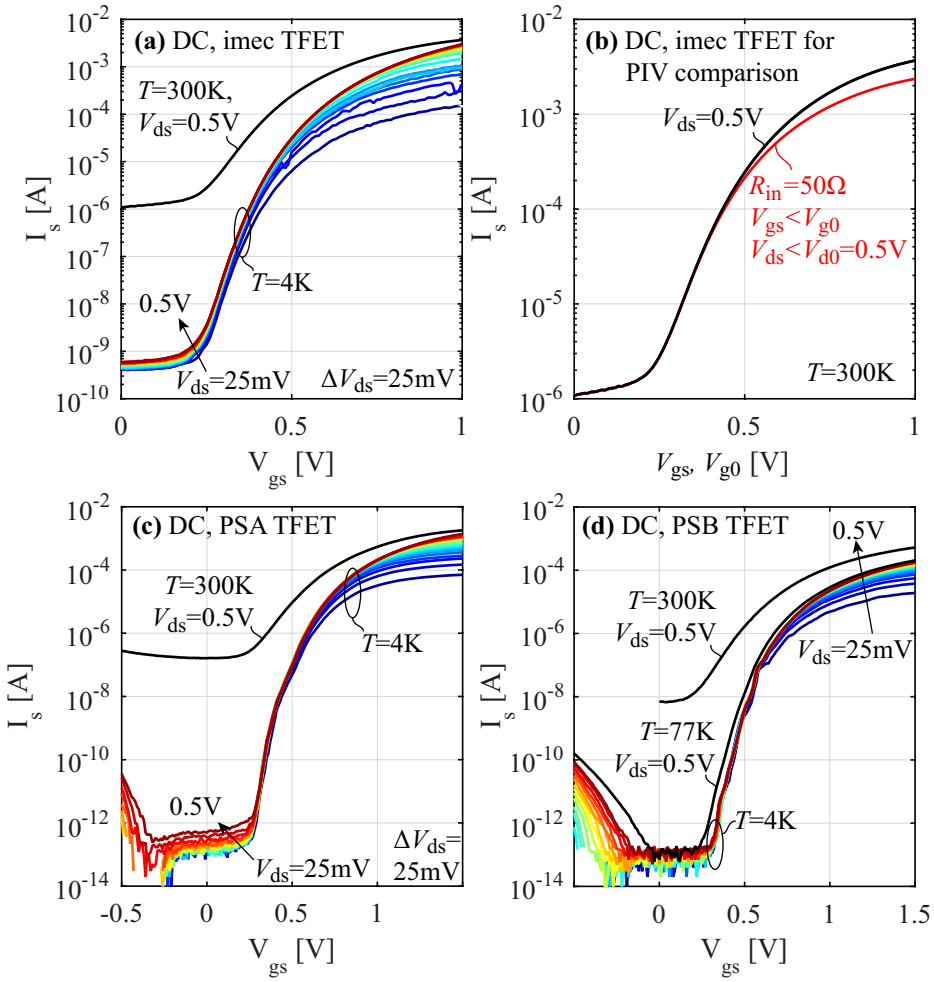


Figure 6.3: The temperature-dependent DC characteristics show a strong decrease in I_{off} for (a) the imec TFET, (c) the PSA TFET and (d) the PSB TFET. This suggests SRH and/or TAT leakage in the off-state. (b) New DC characteristics are calculated for comparison with PIV.

pulsing of the gate voltage impacts SRH generation, because the SRH current increases with V_{gs}.

For the PSA TFET, Datta *et al.* presented temperature dependent *I-V* measurements in the range between 233 K and 300 K [135]. The extracted activation energies suggest dominant SRH at the source/channel heterojunction interface for $V_{gs}<0.1$ V , dominant TAT due to traps at the channel/oxide interface in the range $0.1\,\text{V}<V_{gs}<0.7\,\text{V}$, and dominant BTBT for $V_{gs}>0.7$ V. We will investigate whether we can suppress either the SRH or the TAT current components using pulsed *I-V*.

There is a large variability between different TFETs on the same wafer. For the imec device, the standard deviation is 15 % of the average I_{on} (V_{gs}=1 V, V_{ds}=0.5 V) and 61 % for I_{off} (V_{gs}=0 V, V_{ds}=0.5 V), measured over 16 devices. For PSA the variability is 77 % for I_{on} (V_{gs}=1.5 V, V_{ds}=0.5 V) and 154 % for I_{off} (V_{gs}=0 V, V_{ds}=0.5 V), measured over 10 devices. For PSB it is 64 % for I_{on} and 58 % for I_{off} for the same biases. Within each plot, all measurements are performed on the same device.

TFET DC hysteresis measurements indicate charge trapping at the gate oxide. The characteristics in figure 6.3(a-d) are measured from low to high V_{gs}, but a measurement of the imec TFET in the reverse direction (not shown) shifts the characteristics to higher V_{gs} by 50 mV at T=300 K. This corresponds to more negative charges in the oxide that lead to less band bending in the semiconductor during the down-sweep. A similar shift of 40 mV at T=77 K is observed for the PSA and PSB TFETs.

In conclusion, DC hysteresis measurements indicate charge trapping occurs, and the transfer characteristics are stretched out. In figure 6.3(a,b,d), the large decrease in I_{off} when decreasing the temperature from 300 K to 4 K indicates significant degradation of the transfer characteristics due to thermally assisted SRH and TAT leakage current. The 4 K measurements give an indication of the best possible SRH and TAT suppression we can achieve with PIV.

6.7 Pulsed IV circuit configuration

The PIV circuit is shown in figure 6.4(c). All voltages are referenced to the circuit ground V_0 because the source voltage V_s is not equal to V_0. This is caused by an impedance between the source terminal (at V_s) and the circuit ground (at V_0), further discussed in section 6.9.2. Therefore, we use V_{d0} and V_{g0} instead of V_{ds} and V_{gs}.

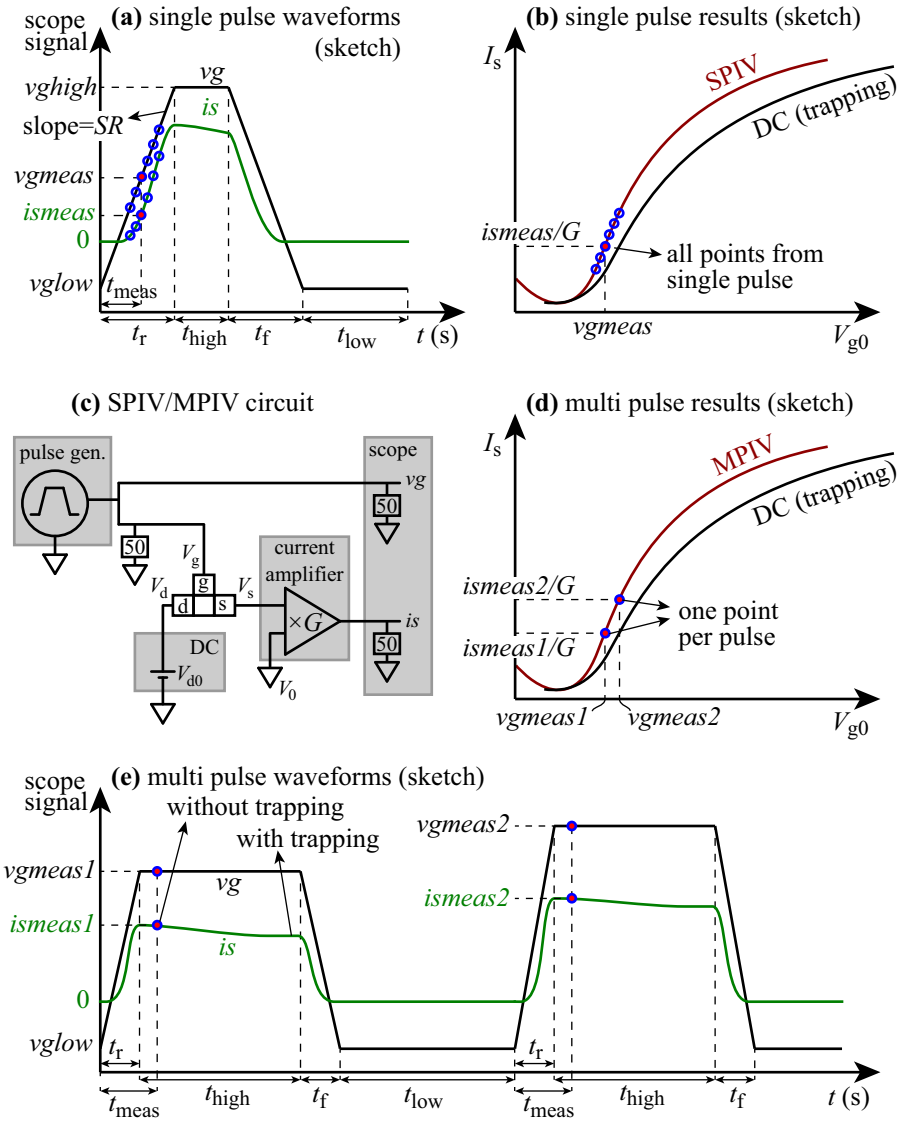


Figure 6.4: All images are sketches, based on measured waveforms in ref. [125]. (a) The SPIV oscilloscope waveforms and (b) results show the data is acquired during the rising (or falling) edges of the pulse. (c) The same circuit configuration is used for SPIV and MPIV. (d) The MPIV oscilloscope waveforms and (d) results show the data is acquired during the top part of the pulse.

To apply V_{g0}, we use an Agilent 81110A pulse generator. It allows rise and fall times (t_r, t_f) down to 2 ns. The signal is split with a 'tee', with one branch to the gate probe and another branch to the oscilloscope to monitor V_{g0}.

The source probe is connected to a *Femto DHCPA-100* current-to-voltage amplifier, which converts the source current I_s to the voltage signal *is*. The amplifier has a variable gain G, and we typically use a setting between 10^2-10^4 V/A. The gain versus bandwidth trade-off of our PIV circuit will be discussed in section 6.9.3. The amplifier couples the input terminal to the circuit ground through a virtual input impedance. The drain probe is connected directly to a *Yokagawa 7651* programmable voltage source, which sets the bias V_{d0}.

The oscilloscopes we use are a *Lecroy Wavemaster 8620A* (6 Ghz bandwidth, 8 bit vertical resolution) and a *Lecroy Teledyne HDO6104* (1 Ghz bandwidth, 12 bit vertical resolution). The t=0 trigger of the oscilloscope is provided by the pulse generator using a separate cable. With the oscilloscope we measure the gate voltage signal (*vg*) and signal representing the source current (*is*). All oscilloscope signals have units of Volts and are written in italics.

In order to reach a high bandwidth and short pulses without distortion, the circuit is impedance matched. The pulse generator is set to 25 Ω output impedance, to have impedance matching at the 'tee'. There, the signal is split into a first branch to the oscilloscope, which is 50 Ω terminated, and a second branch to the gate probe. The TFET gate has a very high input impedance, (>1 GΩ), and impedance matching is achieved by soldering a 50 Ω RF resistor from the gate probe needle to the probe shield. This resistor is shown in the circuit in figure 6.4(c).

To provide a common ground point between the three terminals, we solder a small jumper cable to the source, gate and drain probe shields. This also keeps the current return path physically close to the signal path and lowers inductive impedance in the return current path.

The TFETs are probed using either a *Cascade* probe station or a *LakeShore CPX* probe station for 77 K and 4 K measurements. The full PIV setup at the CPX probe station is shown in figure 6.5.

The pulse generator, DC power suppy and oscilloscope are controlled by a computer with GPIB to automate the PIV measurements. We wrote labview and matlab scripts to automate the pulse generator programming and waveform acquisition, storage and processing. The extraction of a multi pulse I_s-V_{g0} trace with 75 points takes about 30 min, because we require averaging over more than 5000 waveforms for every pulse to suppress noise (section 6.9.1),

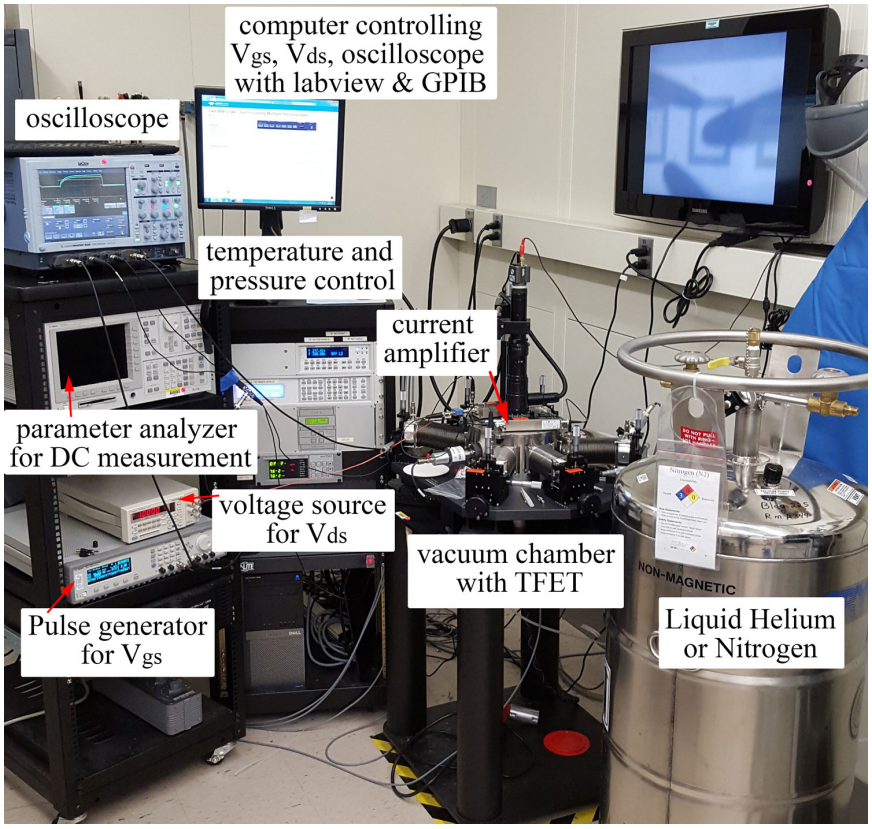


Figure 6.5: The full cryogenic PIV setup with the LakeShore CPX probe station.

6.8 Pulsed IV methods

6.8.1 Single pulse I-V (SPIV)

The single pulse *I-V* (SPIV) method was proposed by Kerber *et al.* [124] from imec in 2003. The sketched waveforms in figure 6.4(a) show the *vg* and *is* signals in the time domain, and the data is extracted during the rising (and sometimes falling) edges of *vg*. For each point in time t_{meas}, the *vgmeas* and *ismeas* data points are mapped to each other, *ismeas* is divided by G, and the data is plotted in figure 6.4(b). The Slew Rate SR=(*vghigh-vglow*)/(t_{r}) in units of V/s is the crucial parameter determining the trapping characteristics.

The method is called 'single pulse' because a complete I_{s}-V_{g0} trace can be

obtained with one pulse, if the oscilloscope has a sufficiently high dynamic range. For our TFET measurements we want to capture both I_{on} and I_{off}, which are typically 5 decades apart. However, the vertical resolution of our 12-bit scope is 2^{12}=4096 points which is insufficient to precisely measure 5 decades of current. Therefore, we have to perform multiple SPIV measurements at different gains G, each one covering a different portion of V_{g0}. We typically take an average of >5000 waveforms to suppress the noise, before extracting the *vgmeas-ismeas* data. We will give an example of the full SPIV measurement procedure in section 6.10.

6.8.2 Multi pulse I-V (MPIV)

Mitard *et al.* from CEA-LETI [126] proposed the multi-pulse method in 2007. It is sometimes also called the "ramped pulse method" [125]. The sketched waveforms in figure 6.4(a) show that for a first (averaged) pulse, a single *vgmeas-ismeas* data point is acquired in the top section of the pulse, at a time where *vg* is constant to avoid the artifact-rich rising edge. A second pulse is then applied with a slightly higher amplitude, and a new *vgmeas-ismeas* data point is extracted, and so on. The *ismeas* values are then divided by G, and the data is plotted in figure 6.4(d). We will propose a modified version of MPIV in section 6.10 to correct for an amplifier DC offset error.

The waveform '*is*' in figure 6.4(e) schematically shows that the current decreases with time due to trapping of charges in the oxide, with a time constant defined in equation (6.1). This sketch is based on measured waveforms in ref. [125]. We can choose arbitrary values of t_{meas} to capture the time evolution of the trapped charge. In section 6.12 we will show that if t_{meas} is taken very large (7 ms), the DC characteristics are recovered.

6.9 Potential measurement errors

Over the course of the PIV measurements, several potential PIV measurement errors were discovered. Some are especially treacherous since the error becomes larger as the slew rate SR increases, which possibly leads to wrong conclusions regarding charge trapping. We give an overview of all pitfalls in figure 6.6.

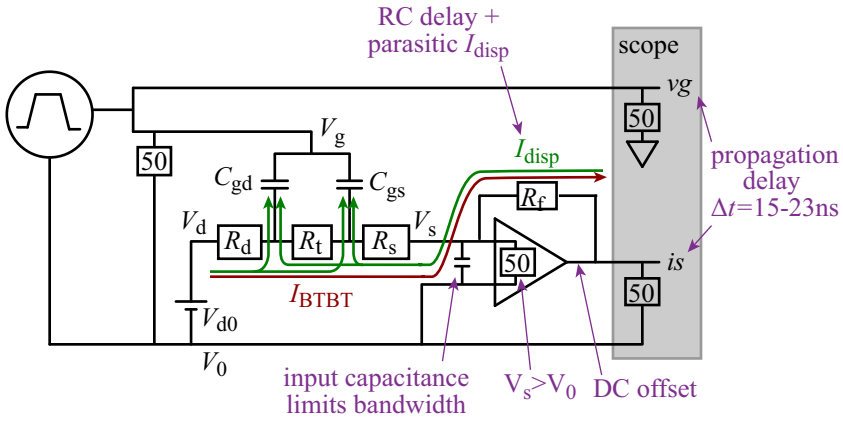


Figure 6.6: Overview of all pitfalls in our PIV measurement circuit

6.9.1 Noise

With the Femto DHCPA-100 variable gain amplifier, we have reached a good compromise between noise, bandwidth and gain by using the following amplifier gains G=10^2, 10^3, 10^4 V/A, with 200, 200 and 80 MHz maximum bandwidth in the high speed setting, or 200, 80, 14 MHz in low noise setting [136].

At the G=10^4 V/A low noise setting, we measure a output peak to peak noise of 5 mV, when capturing a single waveform. This is very high when measuring the TFET's I_{off}=10nA, which corresponds to is=0.1 mV at the oscilloscope. Therefore, we take an average >5000 pulses to reduce the peak to peak noise to 0.2 mV. Then we average the data between t_{meas}-t_{avg}/2 and t_{meas}+t_{avg}/2 with typically t_{avg}=5 to 50 ns. This reduces the peak-to-peak voltage noise to 0.03 mV, which is acceptable compared to the 0.1 mV signal.

6.9.2 Input impedance of amplifier

Our amplifier has an input impedance R_{in}=50 Ω at the G=10^2 and 10^3 V/A settings and 60 Ω at the G=10^4 V/A setting [136]. If we apply V_{g0}=V_{d0}=1 V to the imec TFET, we obtain I_s≈5 mA, and the input impedance leads to a voltage drop of V_{s0}=R_{in} × I_s=0.25 V at the lowest gain setting. Instead of applying the desired 1 V to the TFET, we actually apply V_{gs}=V_{ds}=0.75 V. As we sweep up V_{g0} during a measurement, I_s increases and therefore V_{ds} decreases. The input impedance of the amplifier is shown schematically in figure 6.6 and the problem is labeled as 'V_s>V_0'.

A first solution to prevent this voltage drop is to use a different amplifier which has no input impedance, and is placed close to the TFET (<1-2 cm) to avoid reflections due to impedance mismatch. This involves mounting the amplifier to the probe tip inside the vacuum chamber for cryogenic PIV measurements.

We opted for a second solution, where we account for this voltage drop by modifying the DC characteristics to include R_{in}. This allows us to make a fair comparison with the PIV characteristics. We start with a set of $I_{\mathrm{s}}(V_{\mathrm{gs}},V_{\mathrm{ds}})$ curves measured with HP4156a parameter analyzer, and construct $I_{\mathrm{s}}(V_{\mathrm{g0}},V_{\mathrm{d0}})$ curves by numerical iteration. The final result shown in figure 6.3(b) on p. 137 shows a significant impact of R_{in}=50 Ω on the transfer characteristics.

6.9.3 RC delay

In this section we discuss the impact of RC delay on PIV measurements. We can achieve a higher measurement speed using the MPIV method compared to the SPIV method. This is due to the RC delay which has a larger impact in the SPIV method [126].

The RC delay is the characteristic time constant to charge the gate capacitance and turn on/turn off the TFET. In figure 6.6 we split the gate capacitance in C_{gs} and C_{gd}. In the off-state, R_{t}>1 MΩ, and the charge on C_{gs} is provided by the source contact, and the charge on C_{gd} is provided by the drain contact. Both capacitances need to be fully charged to obtain the full I_{BTBT}. In the on-state, R_{t}<200 Ω and the charge can be provided by either terminal.

The RC delay issue is treacherous. If an increasingly faster slew rate SR is chosen in the SPIV method, or a smaller t_{meas} is chosen in the MPIV method, the TFET is not fully on when the current is sampled, which leads to an increasingly steeper swing. This potentially leads to a wrong conclusion about oxide trapping.

It is easier to visually identify the RC delay in the waveforms of the MPIV method compared to the SPIV method. During the rising edge of the gate pulse in the SPIV method, the BTBT current increases with time due to increasing V_{g0}, but the increase is slower than expected due to the RC delay. It is therefore more difficult to visually recognize the RC delay during the rising edge of the pulse.

We will now make an estimate of the RC delay for the PSA and PSB TFETs. Quantum mechanical simulations of a nano-sized heterojunction $GaAs_{0.5}Sb_{0.5}/In_{0.53}Ga_{0.47}As$ TFET show C_{gs} and C_{gd} are at most 20 aF µm^{-1} (internal results, not yet published). However, the C-V measurements in

figure 6.2(b) show the capacitance of the PSA TFET is much higher. In the off-state, C_{gd}=0.1 pF (from high frequency C^*_{gd}) and C_{gs}=2 pF. In the on-state, C_{gd}+C_{gs}=2 pF. These experimental values are much larger than the quantum mechanical simulations, because the experimental TFET have much larger gate overlap dimensions, and have parasitic contact pad capacitances.

The resistance is given by a combination of the source and drain resistances R_s, R_d, which charge C_{gs} and C_{gd}, but also the feedback resistor R_f in the operational amplifier through which the source current flows (figure 6.6).

For the PSA TFET, we predict that the RC delay is largest in the off-state, when we require the highest amplifier gain, and R_f is highest. All the current charging C_{gs} is provided by the source side, where the feedback resistor R_f=10 kΩ is dominant in case of G=10^4 V, and we obtain RC≈20 ns.

For the imec TFET, the *C-V* measurements in figure 6.2(b) show a much higher maximum capacitance C_{gs}+C_{gs}=60 pF. Therefore we expect the RC delay to be higher. From the measurements in section 6.11 we observe RC=100ns in the on-state.

6.9.4 Amplifier bandwidth

The fastest PIV measurements are achieved by omitting the amplifier and connecting the source directly to the oscilloscope, and use the 50 Ω input resistance to convert the current I_s to a voltage *is*. In literature t_{meas}≈5 ns has been achieved in a similar way [125]. However, the TFET I_{off} (*ismeas*=0.5 µV for I_s=10 nA) would be too small to measure with the oscilloscope, which has a typical measurement range in millivolts. Therefore we need to use a current amplifier.

When selecting an amplifier gain G=10^4 V/A in the high speed setting, the amplifier bandwidth is 80 MHz if the input capacitance <10 pF [136]. For the imec TFET, we have an estimated 30 pF capacitance for the 30 cm cable between the TFET and the amplifier, and C^*_{gs}=60 pF in the on-state. The estimated total input capacitance of 90 pF limits the amplifier bandwidth to 30 MHz, which in turn limits the slew rate of the source current signal. In case of SPIV with SR>1 V/200 ns, we have observed the limited bandwidth leads to a distorted current pulse (not shown). In case of MPIV, we should limit t_{meas}>15 ns [136].

6.9.5 Displacement current

The displacement current I_{disp} is the current that charges and discharges C_{gs} and C_{gd} during the pulse rise time and fall time. Figure 6.6 shows I_{disp} in green, and part of it flows through the source terminal. It is therefore a parasitic current during the I_{BTBT} measurement.

In the off-state, when R_{t} is very high, we calculate $I_{\mathrm{disp}}{=}C_{\mathrm{gs}}{\times}SR$. For the PSA TFET with $C_{\mathrm{gs}}{=}2\,\mathrm{pF}$ and with $SR{=}1\,\mathrm{V}/100\,\mathrm{ns}$, we obtain a predicted $I_{\mathrm{disp}}{=}20\,\mu\mathrm{A}$. We perform SPIV measurements on the PSA TFET and we obtain $I_{\mathrm{disp}}{=}27\,\mu\mathrm{A}$, which is close to the prediction. For the imec TFET we measure $I_{\mathrm{disp}}{=}1.8\,\mu\mathrm{A}$ in the off-state. For both devices, the parasitic I_{disp} is much larger than the typical off-state $I_{\mathrm{BTBT}}{\approx}10\,\mathrm{nA}$ at room temperature, which is problematic.

We can attempt to remove the displacement current contribution by capturing a first '*is(vd0.5)*' waveform at the target $V_{\mathrm{d0}}{=}0.5\,\mathrm{V}$, a measurement that contains $I_{\mathrm{BTBT}}{+}I_{\mathrm{disp}}$. Then we capture a second '*is(vd0)*' waveform at $V_{\mathrm{d0}}{=}0\,\mathrm{V}$, a measurement that contains only I_{disp}. We then subtract the second waveform from the first to extract only I_{BTBT}.

A first issue with this correction method, is the subtraction of two large numbers when $I_{\mathrm{disp}} \gg I_{\mathrm{BTBT}}$. When SR is faster, the displacement is larger and the potential measurement error is therefore larger. This error could be confused with oxide trapping.

As a second issue, we expect I_{disp} to be different at $V_{\mathrm{d0}}{=}0\,\mathrm{V}$ and $0.5\,\mathrm{V}$, because the electrostatic potential distribution in the device changes with V_{d0}, and therefore C_{gs} and C_{gd} also change with V_{d0}. Nevertheless, we will apply this correction method to. SPIV measurements on MOSFET in section 6.10 and we obtain good results. We also apply it to the imec TFET in section 6.11 but we obtain inconsistent results. This is possibly due to the asymmetric C_{gs} and C_{gd} of the TFET, obtained from C-V measurements in figure 6.2.

6.9.6 Propagation delay between *vg* and *is* pulses

Compared to *vg*, the *is* pulse propagates along a longer path, especially because it passes through the amplifier. Therefore it arrives at the oscilloscope with a pulse propagation delay Δt. If this delay is not corrected, values of $V_{\mathrm{g}}(t_{\mathrm{meas}})$ are mapped to $I_{\mathrm{s}}(t_{\mathrm{meas}}{+}\Delta t)$.

For our circuit, Δt is between 15 ns and 23 ns, where the higher value is valid for the higher amplifier gain setting. These values are obtained by calibration

using a 500 Ω RF resistor as a Device Under Test (DUT), which is expected to display a linear I-V dependence.

When performing the SPIV method on a TFET, an improperly corrected Δt leads to a false hysteresis between the rising and falling edge data. The Δt issue is also treacherous, because for a faster SR, the false hysteresis becomes larger, and could be confused with charge trapping. The MPIV method is less sensitive to the Δt issue, because *ismeas* is extracted in the top region of the pulse, where the current changes relatively slowly with time (figure 6.4(a,e)).

6.9.7 DC offset at amplifier output

Most current to voltage amplifiers have a DC offset at the output. It is typically several millivolts, which is large compared to our off-state *ismeas*=0,1 mV predicted in section 6.9.1. If we do not account for this, it also leads to a large measurement error.

We propose a procedure where the DC offset is corrected by performing two PIV measurements. The first one is performed at target $V_{d0} = 0.5\,V$ and second at $V_{d0} = 0\,V$. For the latter, $I_{BTBT} = 0$, and only displacement current is present during rise and fall times. Since both measurements include the same amplifier DC offset, it can be corrected by subtracting the second measurement from the first. We perform this procedure in both MPIV and SPIV measurements in section 6.10. For the latter, this also corrects the displacement current, although not perfectly (as discussed in section 6.9.5).

6.9.8 Overview of MPIV advantages compared to SPIV

- MPIV measurements are less noisy, because we can average the data over a small time period t_{avg}.
- In MPIV, we can choose $t_{meas} \gg$ RC to mitigate the RC delay impact.
- In MPIV, the displacement current issue is avoided entirely, because t_{meas} is taken at the top of the pulse, where *vg* is constant with time.
- MPIV is less sensitive to the pulse propagation delay between both signals, because t_{meas} is taken in a region where *is(t)* changes slowly with t, compared to SPIV.

6.10 Verification using nearly defect free MOSFET

We verify both the SPIV and MPIV with DC offset correction procedure using a Silicon n-MOSFET with a nearly defect free SiO_2 gate oxide. The EOT is 3 nm, the gate length is 160 nm and the electrical width W=15 µm.

We start with the SPIV method. Due to the limited oscilloscope resolution, we start with acquiring the lower part of the I_s-V_{g0} trace in figure 6.7(b), with the amplifier gain set to G=10^4 V/A. Figure 6.7(a) shows several measured waveforms that correspond to this lower part. In a first measurement, the MOSFET is biased at V_{d0}=0.5 V. The gate bias is labeled as *vg*, which we scaled by 1/10 to make the plot more clear. The gate is biased at *vglow*=−0.1 V for −10 µs<t<0 µs. During this de-trapping time, the red waveform *is(vd0.5)* is expected to be nearly zero because the MOSFET is in the off-state, but it is 13 mV due to the amplifier DC offset. At t=0 ns, *vg* increases to 0.3 V in 40 ns, which corresponds to a *SR*=1 V/100 ns. *is(vd0.5)* increases due to the displacement current and the source-drain current. For t>40 ns, during the top portion of the pulse, only the source-drain current is measured.

In a second measurement, the MOSFET is biased at V_{d0}=0 V. The applied pulse (blue *vg* waveform) is identical, but the yellow *is(vd0)* waveform in figure 6.7(a) contains only the displacement current. The yellow waveform is subtracted from the red waveform to obtain the purple waveform *is(vd0.5)-is(vd0)*, which represents only the source-drain current, and has a corrected DC offset. During the rising edge of the *vg* pulse, every value of *vg* is mapped to the value of *is(vd0.5)-is(vd0)* at the corresponding time. We calculate I_s=*(is(vd0.5)-is(vd0))/G* with G=10^4 V/A and we plot this in figure 6.7(b), as shown by the arrow. We have now constructed the first, lower part of this I_s-V_{g0} trace.

A second part of the I_s-V_{g0} trace is constructed with a third and fourth measurement. We set *vglow*=−0.1 V and *vghigh*=0.5 V while keeping *SR*=1 V/100 ns, and we adjust the oscilloscope range to capture the full waveform. In a fifth and sixth measurement, we set *vglow*=−0.1 V and *vghigh*=1 V and adjust the amplifier gain to G=10^3 V/A to prevent current saturation.

During post-processing, we correct for the pulse propagation delay between *is* and *vg* by manually choosing the Δt values. They are chosen such that the different parts of the curve are 'stitched' together in figure 6.7(b). Although we measure significant noise near the off-state, we obtain a satisfactory agreement between the SPIV and the DC characteristics. This is expected because the SiO_2 gate oxide is nearly defect free.

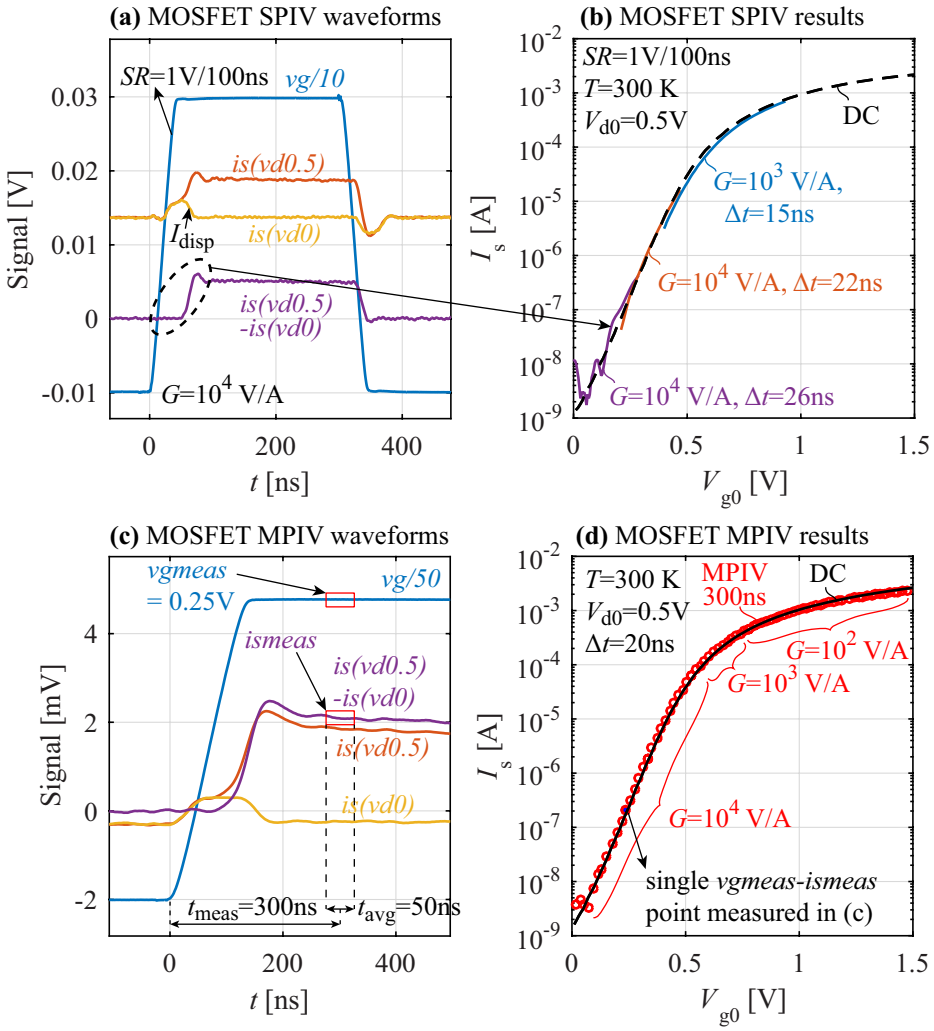


Figure 6.7: Verification of (a-b) single pulse and (c-d) multi pulse I-V methods using Silicon MOSFET with nearly defect-free SiO_2 gate oxide. vg is divided by either 10 or 50 to make the plots more clear.

For the MPIV measurement, figure 6.7(c) shows the measurement procedure is the same as with SPIV. Both *is(vd0.5)* and *is(vd0)* are acquired. Note the different y-axis scale and the different *vg* scaling factor of 1/50 to make the plot more clear.

The *vgmeas* and *ismeas* data points are extracted at a time t_{meas}=300 ns, in the top region of the pulse. The data is averaged over a time t_{avg}=50 ns, which is shown by the red boxes. We then obtain a single data point V_{g0}=*vgmeas* and I_{s}=*ismeas*/G in figure 6.7(d). For this measurement, we have chosen an arbitrary rise time t_{r}=100 ns. In other measurements we have verified that we obtain the same results using e.g. t_{r}=2 ns. The MPIV results in figure 6.7(d) show a near-perfect agreement with the DC characteristics. This is expected and validates the MPIV method.

6.11 TFET PIV measurement results

6.11.1 SPIV measurement

We perform the SPIV method on the imec TFET and we do not obtain consistent results, as shown in figure 6.8(a-b). Using a slew rate SR=1 V/100 ns, the off-state current is underestimated for G=10^2, 10^3 V/A but overestimated for G=10^4 V/A. We suspect this is due to a large RC delay, and a different displacement current at V_{d0}=0 V and V_{d0}=0.5 V. Due to these issues, we focus only on MPIV measurements.

6.11.2 MPIV Measurement parameters

In all TFET MPIV measurements, the de-trapping bias conditions are as follows: the gate is biased at *vglow*=−0.1V for a time t_{low} typically 10-15× longer than pulse time t_{high}, and the drain voltage is constant with V_{d0}=0.5 V. We verify and confirm that taking t_{low}=10^4×t_{high} does not impact the results. For the fastest measurements, we choose t_{low}=10 µs and t_{high}=700 ns. We use rise and fall times t_{r}=t_{f}=2 ns or 100 ns, and we verify and confirm this choice has a negligible impact (not shown).

During low temperature MPIV measurements, which take about 30 min per I_{s}-V_{g0} trace, sometimes the ohmic contact between the probe and the contact pad is broken. We then remove these data points from the plot. Sometimes the contact pad is destroyed. Therefore not all measurement in this chapter labeled e.g. 'PSA' are performed on the same device. However, comparisons of

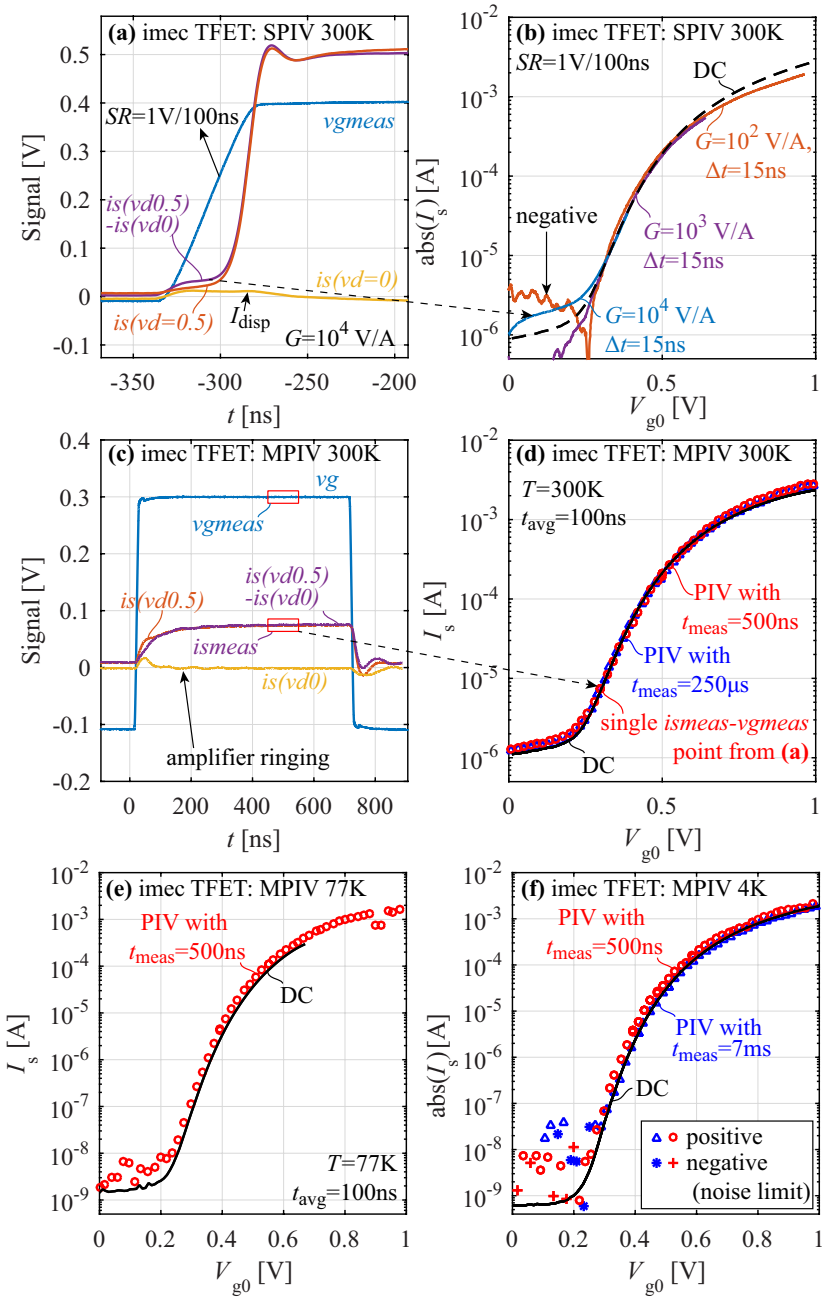


Figure 6.8: (a-d) SPIV measurements for the imec TFET show inconsistent results. (c-f) MPIV results at 300, 77, 4 K show only a minor shift of the characteristics. The + and * symbols in the figure are negative current values, and therefore indicate the MPIV noise limit of 10nA. The devices are possibly different than in figure 6.3.

DC and PIV are done on the same device. All DC measurements are modified to include a 50 Ω series resistance at the source, changing V_{ds} to V_{d0} and V_{gs} to V_{g0}, to make a fair comparison with MPIV measurements (section 6.9.2).

6.11.3 Imec TFET MPIV measurement results

The imec TFET MPIV measurements are shown in figure 6.8(c-f). We observe a large RC delay of ≈100 ns from the purple *is(vd0.5)-is(vd0)* waveform in figure 6.8(c). Therefore we choose t_{meas}=500 ns and t_{avg}=100 ns, indicated by the red boxes, for all imec TFET MPIV measurements. We suspect the large RC delay is caused by the large C^*_{gd}=60 pF measured in figure 6.2 on p. 136.

At room temperature (figure 6.8(d)), we observe that the pulsed I_s with t_{meas}=500 ns is 20% larger compared to DC, for V_{g0}=1 V. For t_{meas}=250 µs, it is only 10% larger the DC value. The intermediate region near V_{g0}=0.5 V is not affected by the pulsing. In the off-state, the pulsed I_s is also 15% larger than the DC I_s. In section 6.12 we will discuss whether the current actually increases for PIV, or if this is rather due to a voltage scale contraction of the characteristics.

When the temperature is lowered to 77 K and 4 K, the DC characteristics show a large decrease in I_{off}, but the MPIV characteristics with t_{meas}=500 ns are quite similar (figure 6.8(e-f)). The MPIV on-state voltage seem shifted by only -50 mV compared to DC. When t_{meas} is increased from 500 ns to 7 ms, the MPIV and DC characteristics match exactly. The + and * symbols in the figure are negative current values, and therefore indicate the MPIV noise limit of 10nA.

6.11.4 PSA and PSB TFET MPIV measurement results

The PSA TFET MPIV measurements are shown in figure 6.9. The purple *is(vd0.5)-is(vd0)* waveform in figure 6.9(a) shows the RC delay of the PSA TFET is smaller (<50 ns) than for the imec TFET due to the lower C_{gs} and C_{gd}. At room temperature, there is near-perfect agreement between the MPIV and DC characteristics, as shown in figure 6.9(b). When lowering the temperature to 77 K and 4 K, there is also a surprisingly good agreement with the DC characteristics, except for a small V_{g0} shift of -60 mV near V_{g0}=1.5 V.

We attempt to make faster MPIV measurements by considering only the on-state, where the RC delay is smaller and the amplifier bandwidth is higher. Figure 6.9(c) shows this allows us to push t_{meas} to 65 ns and 15 ns, but we do not observe a significant steepening of the swing compared to DC.

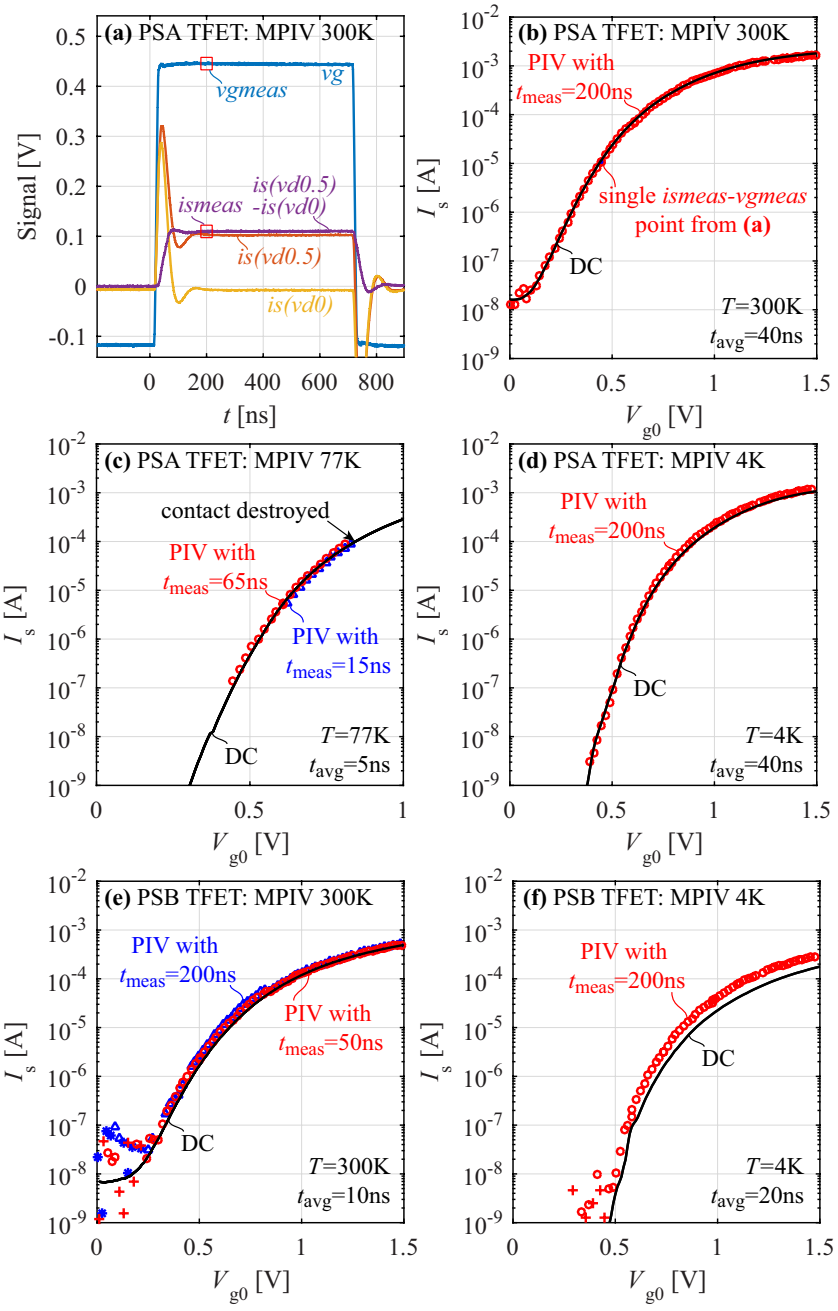


Figure 6.9: Compared to DC, MPIV measurements on (a-d) the PSA and (e-f) the PSB TFET show no improvement of the transfer characteristics at room temperature, and a V_{g0} shift at T=4 K. The devices are possibly different than in figure 6.3.

The PSB TFET MPIV measurements at room temperature are not improved compared to the DC characteristics (figure 6.9(e)), even at t_{meas}=50 ns. However, when the sample is cooled to T=4 K, there is a more significant on-state voltage shift of -220 mV.

6.12 Discussion

We have determined that all our studied TFET contain either interface traps or oxide traps by performing DC hysteresis measurements. We observe a more negative charge trapping when sweeping the gate voltage from high to low V_{g0}. Furthermore, Positive Bias Temperature Instability (PBTI) measurements were performed on the imec TFET in other work [21], and stressing the device for 10 s or longer induced a V_{g0} shift due to charging of oxide traps.

We have also determined that the off-state of all TFETs is highly sensitive to temperature. DC I-V of the PSA and PSB TFETs in figure 6.3(c-d) show that when the temperature is lowered from 300 K to 4 K, I_{off} decreases by nearly 7 orders of magnitude. We observed a similar behavior for the imec TFET in figure 6.3(a). This indicates SRH and/or TAT in the off-state.

We start by discussing the impact of PIV on charge trapping in the TFET off-state in section 6.12.1, and the on-state in section 6.12.2. We then proceed with the impact of PIV on SRH and TAT in section 6.12.3.

6.12.1 Charging of interface/oxide traps in the off-state

Simulations (not shown) indicate the imec TFET transfer characteristics are rather insensitive to interface and oxide traps located near midgap, but much more sensitive to traps located near the conduction band edge and above the conduction band. This is because the electron quasi Fermi level in the channel is located in the upper half of the bandgap in the off-state, and inside the $In_{0.53}Ga_{0.47}As$ conduction band in the on-state. In literature, predictions using equation (6.1) on p. 131 have shown that interaction with interface traps near midgap happens with time constants τ_t between 1 ms and 1 µs [133, 112] at room temperature.

When comparing PIV to DC for the imec TFET in figure 6.8(d), we do not observe a significantly steeper swing in the off-state region. The same is true for the PSA and PSB TFETs in figure 6.9(b,e). Therefore we conclude that either the density of interface traps and oxide traps in the upper half of the bandgap is rather low ($<3 \times 10^{12}$ cm^{-2}) and does not impact the TFET off-state, or the

trapping time constant τ_t is significantly smaller than the prediction and we are unable to suppress trapping with t_{meas}=50 ns.

6.12.2 Charging of interface/oxide traps in the on-state

Simulations show that in the on-state of the imec TFET, the electron quasi Fermi level in the channel is located in the conduction band. Predictions by Vais *et al.* indicate charge carriers interact with interface traps and oxide traps located at this energy level with much shorter time constants, smaller than 1 ns [117]. Trapping deeper in the oxide happens with exponentially longer time constants, up to 1000 s for traps at 3 nm depth [137].

We therefore expect that the MPIV and DC measurements are different in the on-state, and we confirm this in figure 6.8(d). The difference between the MPIV and DC measurement can be perceived either as a lower DC current, or as a V_{g0} stretch-out of the DC characteristics. To determine which of the two possibilities is valid, we first need to determine the on-state conduction mechanism.

For the imec TFET with a 1 nm Al_2O_3/3 nm HfO_2 gate oxide, previously performed temperature dependent DC *I-V* measurements [21] show an activation energy of −13 meV at V_{gs}=1 V, corresponding to a decreased current at higher temperature. This is unusual for TFET, because BTBT is expected to increase due to temperature dependent bandgap narrowing. Furthermore, PBTI measurements in other work have shown a degraded transconductance in the on-state when the device is stressed [21]. Both these arguments strongly suggests that in the on-state, the channel resistance is higher than the tunneling resistance, and the DC current is limited by a degraded channel mobility (coulomb scattering). In literature, PIV measurements of MOSFET have shown that charged interface and oxide traps lead to a similar degradation of the channel mobility [125]. Therefore, the DC on-current of the imec TFET is most likely affected by charge trapping, leading to a both a degraded channel mobility and a V_{g0} stretch-out.

We are able to (at least partially) recover the trap-free on-state current of the imec TFET by PIV. Pulses of t_{meas}=500 ns in figure 6.8(d) show a small improvement in the on-state. This corresponds to an equivalent stretch-out ΔV_{g0}=83 mV of the DC characteristics. We conclude that the room temperature MPIV measurements partially (or completely) suppress interface/oxide trap charging in the conduction band energy range, and this trapping has a time constant τ_t>500 ns.

A phonon-assisted tunneling model for oxide trap charging from Vais *et al.*

[117] shows τ_t is highly temperature dependent. Traps located 0.2 nm from the semiconductor-oxide interface have τ_t=0.6 ns at T=300 K and τ_t=400 ns at T=77 K. An even longer time constant is expected at T=4 K.

When comparing DC and MPIV (t_{meas}=500 ns) measurements for the imec device at T=4 K, we observe a relative stretch-out of ΔV_{g0}=50 mV of the DC characteristics. The stretch-out at T=4 K (50 mV) is smaller than at T=300 K (83 mV), which can be explained by an increased trapping lifetime during the low temperature DC measurement. When the MPIV measurements is performed with t_{meas}=7 ms, it matches with the DC measurement performed in ≈10 s (figure 6.8(f)). This indicates no further charge trapping occurs between 7 ms<τ_t<10 s.

We perform the same analysis on the PSA TFET, which has a 4 nm ZrO gate oxide. We expect dominant BTBT in the on-state from the small and positive activation energy in previous work [135]. PBTI measurements performed in other work [134] show I_{on} is not impacted when stressed up to 1000 s. This confirms dominant BTBT in the on-state.

The PSB TFET, which has a 1 nm HfO_2/3 nm ZrO_2 gate oxide, has a much higher temperature dependence (figure 6.3(d)). I_{on} decreases by a factor 3 when lowering the temperature from 300 K to 77 K, possibly suggesting TAT in the on-state. PBTI measurements performed on the PSB TFET in other work [134] show a severe stretch-out of 350 % when stressed up to 1000 s.

When performing room temperature PIV on the PSA and PSB TFET (figure 6.9(b-e)), there is no significant change compared to the DC characteristics. When performing PIV at T=4 K at t_{meas}=200 ns (figure 6.9(d,f)), we observe an improvement in the on-state: For PSA I_{on}=1 mA is shifted by 60 mV and for PSB I_{on}=0.2 mA is shifted by −220 mV. We conclude that at room temperature, there is a very fast response (τ_t<50 ns) of traps close to or at the interface. Therefore they are not impacted by the PIV measurements. At T =4 K, these traps are slowed down significantly and we observe an improvement of the characteristics. The improvement is largest for the PSB TFET with a 1 nm HfO_2/3 nm ZrO_2 gate oxide. This is consistent with PBTI measurements performed by Pandey *et al.* which show the largest degradation for the PSB TFET [134].

6.12.3 SRH and TAT contributing to increased Ioff

Alian *et al.* reported temperature dependent DC *I-V* measurements of the imec TFET, showing dominant SRH current in the off-state [21]. This current originates either from defects in the large depleted channel of the

device (gate-independent SRH), or from defects in the depleted source/drain regions where the gate overlaps (gate-controlled SRH), or from defects at the semiconductor/oxide interface. From figure 6.8(d), we observe that fast pulsing of the gate with t_{meas}=500 ns does not suppress the increase in SRH current compared to the de-trapping bias condition at V_{g0}. Therefore it is likely that the time constant for the onset of SRH is much smaller than 500 ns.

Temperature dependent DC *I-V* of the PSA and PSB TFETs in figure 6.3(c-d) show a strong decrease in I_{off} of nearly 7 orders of magnitude between 300 K and 4 K. Datta *et al.* reported activation energy measurements on the PSA TFET [135], showing dominant (gate-controlled) TAT for 0.1 V<V_{gs}<0.7 V at T=300 K. We perform room temperature MPIV measurements with t_{meas}=50 and 200 ns to investigate whether we can suppress this increase in gate-controlled TAT current (figure 6.9(b,e)). The results show nearly identical DC and PIV characteristics, therefore additional TAT is not suppressed. Hence it is likely that the time constant for the onset of TAT is <50 ns. This conclusion is not consistent with TFET SPIV measurements performed in other work [44, 18], where a strong TAT decrease was observed for SR>1 V/1 µs. We attribute this discrepancy to the pitfalls in the SPIV method.

6.13 Conclusions and suggestions for future work

We have predicted and observed that single-pulse *I-V* measurements are less robust than multi pulse *I-V* measurements, due to pitfalls like the displacement current correction, RC delay and pulse propagation delay. For single pulse *I-V*, the potential measurement error becomes larger for faster measurements, which is treacherous because it is easily confused with oxide trapping.

We performed multi-pulse *I-V* measurements from room temperature to 4 K on planar homojunction $In_{0.7}Ga_{0.3}As$ TFET from imec. The fast pulse time of 500 ns slightly improves the I_s-V_{g0} characteristics in the on-state. We conclude that charging of interface and/or oxide traps in the conduction band energy range is partially or fully suppressed.

We have also performed pulsed *I-V* measurements on vertical heterojunction $GaAs_{0.4}Sb_{0.6}/In_{0.65}Ga_{0.35}As$ TFET from Penn. State University. Room temperature measurements as fast as 50 ns do not suppress SRH/TAT current in the off-state. Also, these 50 ns pulsed measurements do not suppress V_{g0} stretch-out in the on-state. Literature suggests a time constant <1 ns for traps located at or near the interface and with an energy inside the $In_{0.53}Ga_{0.47}As$ conduction band. Reducing the temperature to 4 K increases the time constant

of these traps, and we succeed in partially or fully suppressing V_{g0} stretch-out with pulsed measurements of 200 ns.

To answer the two first research questions: We are not able to suppress TAT, fast interface and/or oxide trapping by performing room temperature pulsed I-V at 50 ns. We conclude that the time constant for the onset of the TAT is $<$50 ns. Performing a DC measurement at 4 K suppresses SRH and TAT generation, but only partially suppresses charge trapping. We obtain further improvement by performing 4 K pulsed I-V, but we cannot confirm fully trap-free characteristics.

In future work, we recommend applying pulses to both the gate and the drain, to modify the charge state of defects contributing to SRH and TAT and attempt to suppress these mechanisms. Another recommended path is to perform faster measurements ($<$1 ns). These fast measurements can be achieved by reducing C_{gs} and C_{gd} in the TFET, providing Gound-Signal-Ground (GSG) probes, using an amplifier with a higher bandwidth, and mounting this amplifier to the probe tip inside the cryostat.

We also recommend performing quantum mechanical simulations of the PSA and PSB TFETs, for which the dopant profiles can be extracted by SIMS measurements. Comparison of these quantum mechanical simulations with the 'intrinsic' TFET characteristics from cryogenic PIV measurements will allow us to verify if we fully understand the BTBT component in TFETs, and gain additional insight about parasitic effects like band tails due to heavy doping, or heterointerface defects.

Chapter 7

Conclusion and outlook

7.1 General conclusions

Semi-classical and quantum mechanical simulations are crucial to identify promising TFET configurations and guide TFET fabrication. However, at the start of this PhD research in 2011, there was significant uncertainty on the accuracy of many models relevant to TFET and on the corresponding input parameters. Therefore, we performed the experimental calibration of these models.

We calibrated the models for the desired BTBT using $In_{0.53}Ga_{0.47}As$ tunnel diodes. In chapter 2, we have determined that p+/i/n+ diodes are better suited for this purpose than p+/n+ diodes, because the former mitigate uncertainties of sloped dopant profiles and doping dependent bandgap narrowing. We have determined that calibrating BTBT in reverse bias is better than in forward bias, due to the reduced sensitivity to the uncertain Fermi level positions. We identified that an excessive series resistance can result in erroneous calibration, but this issue can be recognized using Esaki diodes. A fixed series resistance shifts the peak voltage, and a spreading resistance lowers the peak current density because not all parts of the diode conduct the same amount of current. Therefore, Esaki diodes are more useful than Zener diodes, because the latter do not have a peak current and peak voltage.

In chapter 3, we have used $In_{0.53}Ga_{0.47}As$ p+/i/n+ diodes for the calibration of BTBT in a semi-classical simulator and a quantum mechanical simulator. For the semi-classical simulator, we have determined that our calibrated BTBT parameters encompass the values predicted by the Kane formalism. This

confirms the validity of direct BTBT models for $In_{0.53}Ga_{0.47}As$, and suggests that reliable predictions can be made for other direct bandgap materials with the existing model. The quantum mechanical simulator is based on the $\mathbf{k} \cdot \mathbf{p}$ formalism. We identified that the coupling energy input parameter (E_P) typically used in 8-band $\mathbf{k} \cdot \mathbf{p}$ implementations is not suited for BTBT modeling, due to the perturbative inclusion of higher bands. Calibrated 2-band, 15-band and 30-band implementations do correctly describe BTBT. These have been used in other work [97] to predict the $In_{0.53}Ga_{0.47}As$ p- and n-TFET performance, which are both promising compared to Silicon MOSFETs.

We achieved a low uncertainty on the BTBT parameters using an imec-developed calibration method. Firstly, we considered p+/i/n+ diodes with different intrinsic region widths (9, 18 and 46 nm) to calibrate the BTBT parameters over a large range of electric fields (0.2−1 MV/cm). Secondly, we combined SIMS and C-V measurements to accurately determine the electrostatic potential profile. This resulted in a low uncertainty of ±30% on the BTBT rate, at electric fields typical for the TFET on-state (4 MV/cm).

We have proposed a model for the temperature dependence of BTBT at low electric fields, derived from Kane's theory: $I_{BTBT} \propto \exp(c\, T^{1.3})$. We obtain much better agreement with experimental results using this model than with the activation energy model, where I_{BTBT} is modeled as $I_{BTBT} \propto \exp(-E_A/(k_B T))$, which does not have a physical origin. We recommend our model to other TFET researchers who wish to suppress TAT in diodes by lowering the temperature, then extrapolate BTBT to other temperatures.

To achieve a low TFET supply voltage while maintaining the same targeted I_{on} and I_{off}, the use of a $GaAs_{0.5}Sb_{0.5}$/ $In_{0.53}Ga_{0.47}As$ heterojunction is promising due to its staggered bandgap alignment. However, there was a large uncertainty on the effective tunneling bandgap $E_{g,eff}$. Therefore, in chapter 4, we have applied our acquired knowledge of BTBT rates to p+/i/i/n+ hetero-diodes, and we calibrated $E_{g,eff}$ to 0.37±0.05 eV. This result was obtained directly from the tunneling current in this lowly doped heterojunction. Our value is hence more reliable for BTBT predictions than values obtained from bandgaps and electron affinities, where the latter is sensitive to semiconductor-vacuum interface reconstructions.

To use this result in future TFET predictions, the effects of high doping need to be taken into account. High doping modifies the conduction and valence band edges, and hence $E_{g,eff}$ and the BTBT rate. We have proposed a new method to extract $E_{g,eff}$, which does not require the BTBT rate. Our method makes use of an energy filtering mechanism in p+/n++ $GaAs_{0.5}Sb_{0.5}/In_{0.53}Ga_{0.47}As$ Esaki diodes, which induces an unusual exponentially increasing BTBT current in forward bias. This exponential current is present when the intermixing region

at the junction is less than 1 nm, which we confirmed using HR-HAADF-STEM analysis on our diodes. Our results for $E_{g,eff}$ in lowly doped (0.37 ± 0.05 eV) and highly doped (0.21 eV) hetero-diodes are in agreement when considering a reduction of $E_{g,eff}$ according to the widely-used Jain-Roulston dopant dependent bandgap narrowing model. For TFET predictions, , our result suggests that high doping of the source (and the optional pocket) significantly impacts $E_{g,eff}$ and hence the TFET performance. However, there is still uncertainty on the impact of high doping on the density of states and hence the BTBT rate. We suggest examining this in future work.

There was also uncertainty on the impact of Field-Induced Quantum Confinement (FIQC) on TFET. Quantum mechanical simulations predicted that FIQC delays the onset of BTBT [65], but experimental proof was still lacking and many semi-classical TFET simulations did not include this effect. In chapter 5, we have experimentally verified the delayed onset of BTBT by FIQC. We achieved this result using easy-to-fabricate highly doped MOS-CAPs, for which we demonstrated AC inversion by BTBT for the first time. These so-called BTBT MOS-CAPs allow the measurement of the first quantized energy level, the onset voltage of line-TFET, and they are promising for the characterization of traps deep into the conduction band.

In order to gain insight in the parasitic current contributions in TFETs, we have calibrated SRH and TAT models due to bulk defects. We have observed that the SRH carrier lifetime is dopant dependent by considering $In_{0.53}Ga_{0.47}As$ p+/n+ diodes and p+/i/n+ diodes. In future work, the possibility of trap-assisted Auger recombination instead of SRH recombination needs to be investigated. Calibrated $In_{0.53}Ga_{0.47}As$ homojunction point-TFET simulations show bulk SRH occurs mainly in the depleted source and drain regions, which are highly doped hence the SRH lifetime is shortest. However, when the gate/source and gate/drain overlap regions are sufficiently short (<500 nm), the bulk TAT and SRH contributions are both negligible (<50 pA µm^{-1}), even when considering the uncertainty about trap-assisted Auger recombination. Therefore it is likely that the high SRH/TAT in most experimental lattice matched $In_{0.53}Ga_{0.47}As$ TFET is not caused by bulk defects but instead by interface defects.

Finally, in chapter 6, we have performed cryogenic multi-pulse *I-V* (MPIV) measurements on planar homojunction $In_{0.7}Ga_{0.3}As$ nTFETs and vertical heterojunction $GaAs_{0.4}Sb_{0.6}/In_{0.65}Ga_{0.35}As$ nTFETs to investigate parasitic oxide trap charging and parasitic SRH/TAT generation. Room temperature MPIV measurements as fast as 50 ns did not suppress SRH and TAT currents. We reduced the temperature to 4 K to increase the time constant of oxide trapping, and we have succeed in partially or fully suppressing V_{gs} stretch-out with pulses of $50-200$ ns. Our MPIV method is more robust than the single-pulse *I-V* method, because the current is measured during the top part of the pulse,

instead of the artifact-rich rising edge of the pulse. These artifacts affect especially the measurement of low off-state currents, which are of interest for TFETs. Therefore the MPIV method is crucial for the accurate characterization of TFETs.

7.2 Suggestions for future work

The road to the industrial implementation of III-V hetero-TFET in integrated circuits remains very challenging. The TFET is targeted for the 5 nm node and beyond, hence we suggest investigating BTBT in highly scaled nanowire diodes. Quantum mechanical predictions show quantum confinement lowers the BTBT current density in nanowire $In_{0.53}Ga_{0.47}As$ tunnel diodes with a diameter smaller than 15 nm. We recommend comparing experimental measurements with quantum mechanical simulations to investigate quantum confinement, random dopant fluctuations [138], deactivation of dopants near the nanowire edges [139, 140], the electrical activity of sidewall defects in MOCVD grown nanowires [38, 141] and sidewall defects in MBE grown and dry etched nanowires [142]. These effects are expected to degrade the TFET performance but their exact impact remains uncertain.

Our research shows that SRH/TAT current due to bulk traps is negligible in lattice-matched MBE-grown $In_{0.53}Ga_{0.47}As$ TFETs. Therefore it is likely that the SRH/TAT current observed in these TFETs in literature is caused by interface defects. We recommend calibrating the SRH/TAT current due to interface defects using TFET and tunnel diodes, and by combining several measurement techniques. We suggest performing additional temperature-dependent PIV measurements and Bias Temperature Instability (BTI) measurements. These are direct and versatile measurement techniques to monitor interface SRH/TAT and the impact of the initial charge state of defects. Also, we suggest performing Deep Level Trap Spectroscopy (DLTS) on tunnel diodes and TFET to monitor the trapped charge, and provide information on the trap energy level and capture cross-section. Combining these measurement techniques with a quantum mechanical implementation of TAT provides a path to fully understand the TAT mechanism and further guide experimental research on TFET gate stack improvement.

Appendix A

Appendix: Sentaurus input files

A.1 SPROCESS input file

Save the code below in a file named `in-sprocess.cmd`. Run with the command `sprocess -rel I-2013.12 in-sprocess.cmd`

```
line x loc=  0.01        tag=tops        spacing=0.0001
line x loc=  0                tag=bot                spacing=0.0001
line y loc=  -0.1        tag=left        spacing=0.2
line y loc=  0.1        tag=right        spacing=0.2
region Silicon   name=sub substrate     xlo=bot xhi=tops ylo=left yhi=right
init
pdbSet Grid SnMesh min.normal.size 0.0001
pdbSet Grid SnMesh normal.growth.ratio.2d 1
grid remesh
mater add name = InGaAs new.like = Silicon
mater add name = GaAsSb new.like = Silicon

doping name=nIGA   field= {Selenium}   depths= {0 0.05} values= {2e19 2e19}
doping name=pIGA  field= {Beryllium}     depths= {0 0.05}  values= {1e16 1e16}
doping name=nGAS   field= {Arsenic}   depths= {0 0.05} values= {1e16 1e16}
doping name=pGAS  field= {Boron}     depths= {0 0.05}  values= {2e19 2e19}

deposit material= {InGaAs} thickness = 0.05 doping= {nIGA pIGA} region.name=region1
deposit material= {GaAsSb} thickness = 0.05 doping= {nGAS pGAS} region.name=region2
```

```
diffuse temp=1050 time=0 !stress.relax
transform translate= {0.1 0 0} ;#change 0.1 to total thickness
transform cut min= {0 -0.2} max= {0.1 0.2} ;#change 0.1 to total thickness
contact name=ncontact bottom
contact name=pcontact box GaAsSb adjacent.material= Gas xlo= -0.1 xhi= 0.1
struct     tdr=out-sprocess
struct   smesh=out-sprocess
exit
```

A.2 SDEVICE command file

Save the code below in a file named `in-sdevice.cmd`. Run with the command `sdevice -rel K-2015.06 in-sdevice.cmd`

```
File{
        Grid         ="out-sprocess_fps.tdr"
        Parameter = "in-sdevice.par"
        Plot          ="out-sdevice.tdr"
        #NonlocalPlot="out-device_nonlocal.plt"
        Current    ="out-sdevice.plt"
        Output = "out-sdevice.log"
        }

Electrode{
        { Name="ncontact"  Voltage=0 }
        { Name="pcontact"    Voltage=0 }
        }

Physics{
        Areafactor=5#brings diode area to 1um2
        Temperature=300
        Fermi
        eMultivalley(NonParabolicity)
        hMultivalley(NonParabolicity)

        ###for BTBT at InGaAs/GaAsSb interface:
        #eBarrierTunneling "NLM_inter"(Band2Band=Full)
        #hBarrierTunneling "NLM_inter"(Band2Band=Full)

        ###for BTBT everywhere:
        Recombination(Band2Band(Model=NonlocalPath1
                -InterfaceReflection -FranzDispersion))

        ###for intraband tunneling at InGaAs/InP interface:
```

```
58          #eBarrierTunneling "NLM_intra"
59          #hBarrierTunneling "NLM_intra"
60
61          #for SRH:
62          #Recombination(SRH(Dopingdependence))
63          #for TAT:
64          #Recombination(SRH(NonlocalPath(Lifetime = Schenk TwoBand Fermi)))
65
66          EffectiveIntrinsicDensity (NoBandGapNarrowing)
67          #EffectiveIntrinsicDensity (NoFermi BandGapNarrowing (JainRoulston))
68          }
69
70  #Physics(MaterialInterface="InP/InGaAs)"{
71  #         Thermionic
72  #         HeteroInterface
73  #         }
74
75  Plot{
76          EffectiveBandgap
77          eDensity hDensity
78          eCurrent hCurrent TotalCurrent
79          SRHrecombination
80          eSRHrecombination hSRHrecombination tSRHrecombination
81          TotalRecombination
82          Potential
83          ElectricField/Vector
84          eBarrierTunneling hBarrierTunneling
85          Band2BandGeneration
86          eBand2BandGeneration hBand2BandGeneration
87          eQuasiFermiEnergy hQuasiFermiEnergy
88          ConductionBand ValenceBand
89          Doping DonorConcentration AcceptorConcentration
90          }
91
92  #NonLocalPlot((0.01 -0.001)){
93  #         eBarrierTunneling hBarrierTunneling
94  #         Wavefunction
95  #         EigenEnergy
96  #         eDensity hDensity
97  #         ConductionBand
98  #         ValenceBand
99  #         eQuasiFermiEnergy hQuasiFermiEnergy
100 #         }
101
102 CurrentPlot{
103         eBand2BandGeneration(Integrate(Everywhere))
```

```
104         hBand2BandGeneration(Integrate(Everywhere))
105         SRHRecombination(Integrate(Everywhere))
106         eSRHRecombination(Integrate(Everywhere))
107         tSRHRecombination(Integrate(Everywhere))
108         hSRHRecombination(Integrate(Everywhere))
109         TotalRecombination(Integrate(Everywhere))
110         }
111
112 Math{
113         ###nonlocal mesh for BTBT at InGaAs/GaAsSb interface:
114         #Nonlocal "NLM_inter" (RegionInterface="region1/region2"
115                 Length=20e-7 Permeation=20e-7 Direction=(0 1 0) MaxAngle=5)
116
117         ###nonlocal mesh for intraband tunneling at InGaAs/InP interface:
118         #Nonlocal "NLM_intra" (Materialnterface="InGaAs/InP"
119                 Length=20e-7 Permeation=20e-7 Direction=(0 1 0) MaxAngle=5)
120
121         Extrapolate
122         RelErrControl
123         Iterations=20
124         Currentweighting
125         Digits=5
126         DensityIntegral(30) #set 150 for T<100 to avoid convergence issues
127         }
128
129 Solve{
130         Coupled {Poisson Electron Hole}
131         Plot(Fileprefix="out-Vnp0.0V" noOverwrite)
132
133         Quasistationary(InitialStep=1e-6 Increment=2 MinStep=1e-6 MaxStep=1
134         Goal { Name="ncontact" Voltage=-0.10} )
135         {Coupled {Poisson Electron Hole}}
136         Plot(Fileprefix="out-Vnp-0.10V" noOverwrite)
137
138         Quasistationary( InitialStep=0.1 Increment=2 MinStep=1e-6 MaxStep=1
139         Goal { Name="ncontact" Voltage=-0.50} )
140         {Coupled {Poisson Electron Hole}}
141         Plot(Fileprefix="out-Vnp-0.50V" noOverwrite)
142
143         NewCurrentFile="out-currentsweep"
144
145         Quasistationary(
146         InitialStep=0.005 Increment=2 MinStep=0.001 MaxStep=0.1
147         Goal { Name="ncontact" Voltage=0.5} )
148         {Coupled {Poisson Electron Hole}}
149         Plot(Fileprefix="out-Vnp0.5V" noOverwrite)
```

```
150         }
```

A.3 SDEVICE parameter file

Save the code below in a file named `in-sdevice.par`

```
151 Material="InGaAs"{
152 Bandgap{
153         Chi0       = 4.46    # [eV]
154         Bgn2Chi= 0.5      # [1]
155         Eg0         = 0.8215  # [eV]
156         alpha      = 0.348e-03   # [eV K^-1]
157         beta       = 80.0000             # [K]
158         Tpar       = 0.0000e+00     # [K]
159         }
160
161 MultiValley{
162         eValley(0.043, 0.043, 0.043, 0, 1, 1.35) #Gamma
163         eValley(0.29, 0.29, 0.29, 0.46, 4, 0.42) #L
164         eValley(0.68, 0.68, 0.68, 0.59, 3, 0.077) #X
165         hValley(0.052, 0.052, 0.052, 0, 1, 0) #mlh
166         hValley(0.450, 0.450, 0.450, 0, 1, 0) #mhh
167         hValley(0.150, 0.150, 0.150, -0.33, 1, 0.0) #so
168         }
169
170 eDOSMass{
171         Formula        = 2        # [1]
172         a        = 0.1905        # [1]
173         ml        = 0.9163        # [1]
174         mm        = 0.0000e+00        # [1]
175         Nc300        = 2e+17        # [cm-3]
176         }
177
178 hDOSMass{
179         Formula        = 2        # [1]
180         a        = 0.443587        # [1]
181         b        = 3.6095e-03        # [K^-1]
182         c        = 1.1735e-04        # [K^-2]
183         d        = 1.2632e-06        # [K^-3]
184         e        = 3.0256e-09        # [K^-4]
185         f        = 4.6834e-03        # [K^-1]
186         g        = 2.2869e-04        # [K^-2]
187         h        = 7.4693e-07        # [K^-3]
188         i        = 1.7275e-09        # [K^-4]
```

```
189         mm         = 0.0000e+00         # [1]
190         Nv300        = 8.0000e+18         # [cm-3]
191         }
192
193 Band2BandTunneling{
194         m_c= 0.045 #[m0]
195         m_v= 0.055 #[m0]
196         degeneracy=1.6
197         Apath= 0
198         Bpath= 0
199         Cpath=0
200         Ppath=0
201         Rpath= 1.21
202         MaxTunnelLength= 100e-7         # [cm]
203         }
204
205 BarrierTunneling{
206         mt = 0.045, 0.055 #[m0]
207         g = 1.6 , 1.6
208         }
209
210 JainRoulston{
211         A_n = 4.76E-8 # [eV cm]
212         A_p = 9.2E-9 # [eV cm]
213         B_n = 1.11E-7 # [eV cm^(3/4)]
214         B_p = 3.5E-7 # [eV cm^(3/4)]
215         C_n = 0 # [eV cm^(3/2)]
216         C_p = 3.4E-12 # [eV cm^(3/2)]
217         D_n = 0 # [eV cm^(3/2)]
218         D_p = 2.3E-13 # [eV cm^(3/2)]
219         }
220
221 Epsilon{
222         epsilon         = 13.9         # [1]
223         }
224
225 Epsilon_aniso{
226         epsilon         = 13.9         # [1]
227         }
228
229 Scharfetter{
230         taumin= 0.0000e+00 ,   0.0000e+00 # [s]
231         taumax=         3E-12,         3E-12         # [s]
232         Nref=         1.0e+16,         1.0e+16         # [cm-3]
233         gamma=         2,                 2         # []
234         Etrap=         0.0e+00# [eV]
```

```
235         }
236
237 TrapAssistedTunneling{
238         S=10# [1]
239         hbarOmega=0.034# [eV]
240         m_theta=0.043,        0.052        # [m0]
241         Z        = 0.0000e+00               # [1]
242         MinField        = 0.0000e+00        # [V/cm]
243         DenCorRef        = 1.0000e+03 ,        1.0000e+03        # [cm^-3]
244         }
245 }
246 ******************************************************
247 Material="InP"{
248 Bandgap{
249         Chi0        = 4.38        # [eV]
250         Bgn2Chi         = 0.5        # [1]
251         Eg0        = 1.344  # [eV]
252         }
253
254 eDOSMass{
255         Formula         = 2        # [1]
256         Nc300        = 5.7e+17        # [cm-3]
257         }
258
259 hDOSMass{
260         Formula         = 2        # [1]
261         a        = 0.443587        # [1]
262         b        = 3.6095e-03        # [K^-1]
263         c        = 1.1735e-04        # [K^-2]
264         d        = 1.2632e-06        # [K^-3]
265         e        = 3.0256e-09        # [K^-4]
266         f        = 4.6834e-03        # [K^-1]
267         g        = 2.2869e-04        # [K^-2]
268         h        = 7.4693e-07        # [K^-3]
269         i        = 1.7275e-09        # [K^-4]
270         mm        = 0.0000e+00        # [1]
271         Nv300        = 1.1000e+19        # [cm-3]
272         }
273
274 MultiValley{
275         eValley(0.08, 0.08, 0.08, 0, 2, 0.63)  #gamma
276         eValley(0.25, 0.25, 0.25, 0.59, 4, 0.29)  #L
277         hValley(0.089, 0.089, 0.089, 0, 1, 0.0) #mlh
278         hValley(0.6, 0.6, 0.6, 0, 1, 0.0)          #mhh
279 }
280
```

```
281 BarrierTunneling{
282         mt = 0.08, 0.089 #[m0]
283         g = 1 , 1
284         }
285
286 Epsilon{
287         epsilon         = 12.5         # [1]
288         }
289
290 Epsilon_aniso{
291         epsilon         = 12.5         # [1]
292         }
293 }
294
295 ******************************************************
296 Material="GaAsSb"{
297 Bandgap{
298         Chi0         = 4.07         # [eV]
299         Bgn2Chi          = 0.5          # [1]
300         Eg0         = 0.77 #[eV]
301         }
302
303 eDOSMass{
304         Formula          = 2         # [1]
305         a         = 0.1905         # [1]
306         ml          = 0.9163         # [1]
307         mm          = 0.0000e+00          # [1]
308         Nc300          = 2.6e+17          # [cm-3]
309         }
310
311 hDOSMass{
312         Formula          = 2         # [1]
313          a          = 0.443587          # [1]
314         b         = 3.6095e-03          # [K^-1]
315         c         = 1.1735e-04          # [K^-2]
316         d         = 1.2632e-06          # [K^-3]
317         e         = 3.0256e-09          # [K^-4]
318         f         = 4.6834e-03          # [K^-1]
319         g         = 2.2869e-04          # [K^-2]
320         h         = 7.4693e-07          # [K^-3]
321         i         = 1.7275e-09          # [K^-4]
322         mm          = 0.0000e+00          # [1]
323         Nv300          = 1.35000e+19          # [cm-3]
324         }
325
326
```

```
Band2BandTunneling{
        m_c= 0.045 #[m0]
        m_v= 0.066 #[m0]
        degeneracy=2 # []
        Apath= 0
        Bpath= 0
        Cpath=0
        Ppath=0
        Rpath= 1.21
        MaxTunnelLength        = 100e-7        # [cm]
        }

MultiValley{
        eValley(0.045, 0.045, 0.045, 0.0000e+00, 1, 1.28) #gamma
        hValley(0.066, 0.066, 0.066, 0.0000e+00, 1, 0.0) #mlh
        hValley(0.455, 0.455, 0.455, 0.0000e+00, 1, 0.0) #mhh
        }

BarrierTunneling{
        mt = 0.045, 0.066 #[m0]
             g = 1 , 1
        }

Epsilon{
        epsilon        = 14.3        # [1]
        }

Epsilon_aniso{
        epsilon        = 14.3        # [1]
        }

JainRoulston{
        *taken from InGaAs
        A_n = 4.76E-8 # [eV cm]
        A_p = 9.2E-9 # [eV cm]
        B_n = 1.11E-7 # [eV cm^(3/4)]
        B_p = 3.5E-7 # [eV cm^(3/4)]
        C_n = 0 # [eV cm^(3/2)]
        C_p = 3.4E-12 # [eV cm^(3/2)]
        D_n = 0 # [eV cm^(3/2)]
        D_p = 2.3E-13 # [eV cm^(3/2)]
        }
}
```

Appendix B

Large diodes without separate contact pads and electrical results

In the first year of this PhD, $In_{0.53}Ga_{0.47}As$ p+/i/n+ diodes with diameters $W_i$in the range 100 µm<W_i<910 µm were fabricated with the purpose of Band-To-Band Tunneling (BTBT) current density extraction and BTBT model calibration. As predicted in section 2.4.6 on p. 48, these large diameters result in a series resistance much larger than the BTBT resistance. This hinders the BTBT current extraction. The process flow and electrical results of these diodes are shown in this appendix for documentation purposes.

The large diode diameter was chosen based on availability of the lithography mask, and ease of fabrication. Due to the large diode diameters, the top contact to the n+ $In_{0.53}Ga_{0.47}As$ layer can be deposited entirely on the mesa, and comfortable placement of measurement probes is possible without requiring the fabrication of separate contact pads with an isolating interlayer.

B.1 Fabrication

The fast fabrication flow for these large diodes is shown in figure B.1. It uses the i-line lithography mask with the name *Diode Test Mask Anne*. First, a p+/10 nm i/n+ $In_{0.53}Ga_{0.47}As$ stack is grown on a p-type InP substrate using Molecular

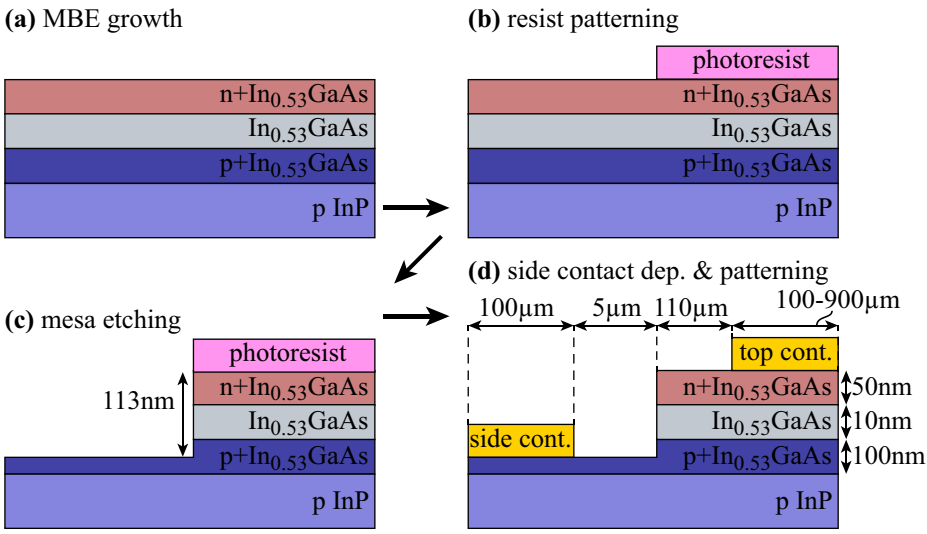


Figure B.1: Fast fabrication flow for diodes with mesa diameters >100 µm, and which therefore do not require separate contact pads.

Beam Epitaxy (MBE) (figure B.1(a)). The doping levels are N_A=8 × 10^{18} cm^{-3} and N_D=1.5 × 10^{19} cm^{-3}, extracted using SIMS. IX845 resist is then patterned using the MESA level (bright field) of the mask (figure B.1(b)). The diode mesa is then etched in a diluted sulfuric acid-peroxide solution to obtain a $In_{0.53}Ga_{0.47}As$ etch depth of 113 nm (figure B.1(c)). The resist is stripped in acetone and the sample is rinsed with IPA. In the final process step, a bilayer stack of LOR1A/IX845 is patterned using the *SHOT* and *OHM* levels (dark field) of the mask. The metal stack 10 nm Ti/30 nm Pt/100 nm Au is then evaporated to make contact to both the p+ and n+ $In_{0.53}Ga_{0.47}As$ layers. The resist is stripped in microstrip MS2001, the samples are rinsed, and finally annealed for 5 min at 400°C. We obtain the result in figure B.1(d).

B.2 Electrical characterization

The temperature dependent *I-V* characteristics are measured with a *HP4156c* precision parameter analyzer from *Agilent* in a *PA300* prober system for $T >$ 300 K and in a *Janis* cryostat for T<300 K. Measurements of diodes with different diameters indicate the current does not scale with the junction area,

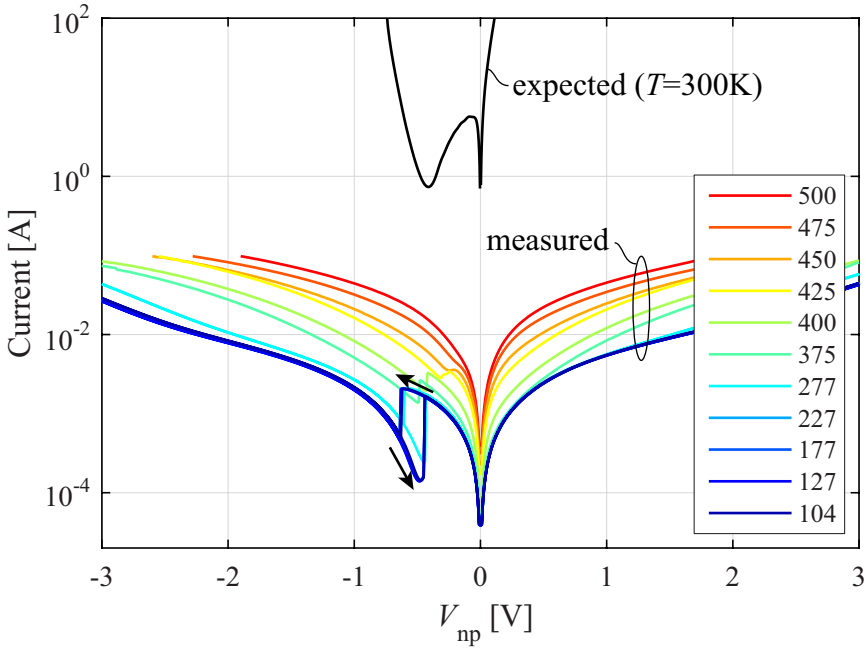


Figure B.2: The colored lines are the I-V characteristics of a p+/10 nm i/n+ $In_{0.53}Ga_{0.47}As$ diode with a diode mesa diameter of 460 µm. The legend shows the measurement temperature in Kelvin. For T<227 K, the I-V curves are measured in both directions, and hysteresis is observed in forward bias. The black arrows show the measurement direction. The expected current is taken from the current density of a p+/9nm i/n+ $In_{0.53}Ga_{0.47}As$ diode in figure 3.4(c) with a much smaller diameter (4.3 µm), and scaled to 460 µm. For this diode with small dimensions, the impact of parasitic series resistance is negligible.

and the electrostatic potential is not uniform over the junction area (electrical results not shown).

The temperature dependent I-V traces for one diode with junction diameter 460 µm are shown by the colored lines in figure B.2. The black line shows the expected I-V trace, calculated from a much smaller diode with nearly the same MBE stack. The measured current for the diode with 460 µm is order of magnitudes than the expected current, due to a large potential drop over the spreading resistance.

There is a strong temperature dependence for T>227 K, indicating that the flow of majority carriers is limited by thermionic emission. For T<227 K,

there is no temperature dependence, indicating direct tunneling only. We attribute this to an insufficiently thick p+ $In_{0.53}Ga_{0.47}As$ layer, leading to a large spreading resistance. The current does not flow efficiently through the InP substrate either, due to the presence of an electrostatic potential barrier at the $In_{0.53}Ga_{0.47}As$/InP heterojunction, as shown in figure 2.12(a) on p. 46.

For $T<227\,K$, the I-V characteristics are measured in both voltage directions, and hysteresis is observed in forward bias (black arrows in figure B.2). This bistable operation can be explained by the Esaki diode NDR characteristics, in series with the large nonlinear series resistance due to the heterojunction, as predicted in figure 2.15(d) on p. 50. Therefore we cannot use these distorted I-V characteristics for BTBT calibration.

Appendix C

Esaki diode fabrication

In section 2.4.6 on p. 48, we have set requirements for the dimensions of $In_{0.53}Ga_{0.47}As$ p+/10 nm i/n+ Esaki diodes on p-InP substrates. These are: a diode junction area of A_j=0.5 µm^2, a p+$In_{0.53}Ga_{0.47}As$ layer thickness of t_{ptype}=600 nm, and a side contact spacing $L_{spacing}$=0.1 µm. In this appendix, we develop a new process flow for the fabrication of $In_{0.53}Ga_{0.47}As$ tunnel diodes, according to these requirements. The fabrication flow for $In_{0.53}Ga_{0.47}As$/ $GaAs_{0.5}Sb_{0.5}$ heterojunction diodes is similar, and the specifics are summarized in chapter 4.

We start with an overview of the process flow in section C.1. We design the lithography mask in section C.2. The Molecular Beam Epitaxy (MBE) growth of the stacks, the hard mask patterning and the diode mesa etching are discussed in sections C.3-C.7. We discuss the measurement of the mesa dimensions in section C.8

The contact modules to the p+$In_{0.53}Ga_{0.47}As$ and n+$In_{0.53}Ga_{0.47}As$ are discussed in sections C.9-C.14. For the contact to the p+ $In_{0.53}Ga_{0.47}As$, we have the possibility of depositing a metal directly on the p+$In_{0.53}Ga_{0.47}As$ layer, or depositing a metal on the back of the substrate. We have previously discussed these two contacting schemes in section 2.4.6. Each scheme has its own benefits, therefore both are developed.

In the first year of this thesis, a different, more simple fabrication flow was used for $In_{0.53}Ga_{0.47}As$ p+/i/n+ diodes with large junction diameters >100 µm, which do not require separate contact pads. The flow and the corresponding electrical results are documented in appendix B but cannot be used for BTBT calibration due to the excessively large diode dimensions.

C.1 Fabrication flow overview

Figures C.1 and C.2 schematically show the new fabrication flow for $In_{0.53}Ga_{0.47}As$ diodes. The geometry of the diodes is defined by a patterned SiO_2 hard mask (figure C.1(b)) and wet etching (figure C.1(d)). This hard mask is sacrificial, because it is later replaced by the top contact in figure C.2(i). This large $50\times50\,\mu m^2$ top contact is connected to the top surface of the much smaller diode, but electrically isolated from the underlying semiconductor using the interlayer dielectric Benzocyclobutene (BCB). The fabrication flow offers the possibility to deposit either a back contact to the substrate (figure C.1(c)), or a self-aligned side contact on the wet etched semiconductor (figure C.1(e)), or both. Finally, the fabrication flow features 40 different target dimensions, to investigate whether or not the current scales with the tunneling junction area. There are three different diode shapes (round, square, diamond) to investigate the impact of the exposed crystallographic planes on defect-based perimeter current.

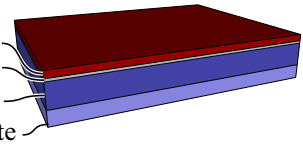
This fabrication flow is developed by combining the following ideas: The idea of sacrificial hard mask and BCB planarization originates from Zheng *et al.* [82]. The idea of a self-aligned side contact originates from the self-aligned gate in the TFET by Mohata *et al.* [143]. Process steps (b), (d), (e), (g), (h), (i) and (j) are either not optimized or not available in the imec clean room. The development of these steps is discussed in the following sections, starting with the design of the lithographic masks.

Figures C.1 and C.2 show the optimized recipe to fabricate sub-micron diodes with contact pads using the tools and recipes available in the imec clean room called 'III-V lab'. If the reader would like to replicate this recipe using different tools, all etch recipes should be re-calibrated. For some process steps, two possible options are listed. The recommended option (the easiest and fastest) is indicated in figures C.1 and C.2, but more details about the advantages of both options are provided in the text below.

C.2 Lithography mask design

The mask set is designed using the program *Clewin4.exe* and is shown in figure C.3 . It consists of two levels (two lithography steps). The first MESA level, which defines the hard mask and diode mesa shapes, is performed using e-beam lithography. This process step is shown schematically in figure C.1(b). The MESA level contains three shapes with target width W_i. The Round (R) shape has a diameter W_i, the square (S) shape has a side length W_i, and the

(a) MBE growth

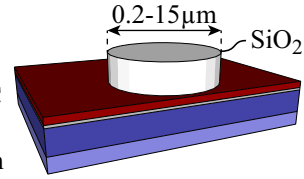


(b) Hard mask patterning

- HCl:H_2O 1:5 10s dip
- N_2O plasma preclean
- 300nm CVD 350°C SiO_2 (33.3min at 9nm/min)
- ma-N 2403 30s@2000 rpm
- 30min bake at 110°C
- MESA e-beam exposure 60 or 200μC/cm2
- develop 150s in ma-D 525
- 2min H_2O rinse
- dry etch recipe (j) in fig.C.6

OR (recommended)

- FOX12 60s spin at 900rpm
- bake 40min at 90°C
- MESA e-beam exp.
- develop 60s Si etch 10s rinse in OPD262:H_2O 1:10
- N_2 dry

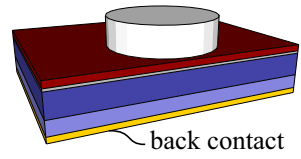


(c) Back contact deposition (optional)

- spin protective resist IX845 frontside
- 30nm AuZn/70m Au evaporation
- 60s acetone rinse + 60s IPA rinse + N_2 dry
- 5min anneal at 400°C in N_2 ambient

OR (recommended)

- sputter Mo/Al on InP backside after step (j)

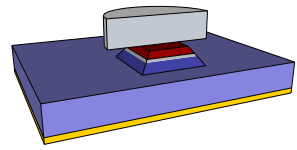


(d) Diode wet etching

- citric acid:H_2O_2:H_2O 5:5:1600 2400s for 180nm target etch depth

OR

- sulfuric acid:H_2O_2:H_2O 1:3:1000 800s for 200nm target etch depth



(e) Side contact deposition (optional)

- evaporation of 3nm Pd/3nm Ti/ 20nm Pd/30nm Au/ 5nm Ti

OR

- 20nm Mo/30nm Al

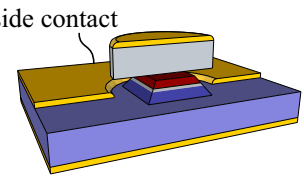
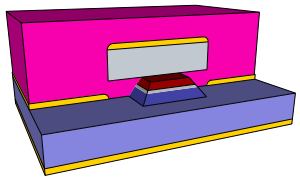
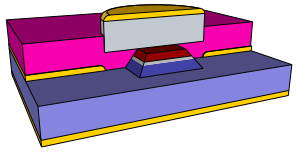


Figure C.1: Part one of the optimized fabrication flow for sub-micron sized diodes with separate contact pads.

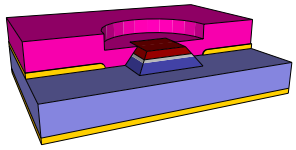
(f) BCB spinning and curing
- spinning of BCB3022-46
  60s@3000rpm for 2.9µm target
- cure in vacuum oven with
  temperature ramping as in section C.10



(g) BCB recess
- dry etch RIE 180sccm O_2, 50sccm SF_6,
  300mtorr, 150W
  about 150s for 2.6µm target etch
  etch in steps, monitor thickness with
  profilometer and reflectometer



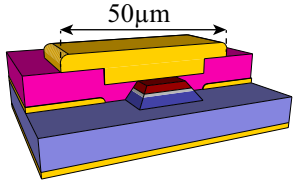
(h) Top contact opening
- if (e) was performed:
  30 steps of 30s Xe ion milling
  for side contact removal
- 30s BHF for SiO_2 removal



(i) Top contact dep. & pattern
- 20nm Mo/150nm Au sputtering
- LOR1A std.+ IX845 std.
- i-line litho TOPCONTACT bright field
- 25 steps of 30s Xe ion milling
- 10min MS2001 at 82°C+10min ultrasonic
- IPA +H_2O showerhead rinse

OR ↓ recommended

- 20nm Mo/150nm Al sputtering
- IX845 std.
- i-line litho TOPCONTACT (opt. protective resist backside)
- OPD5262 until Al removed (visual check)
- H_2O_2 until Mo removed (visual check)



(j) Side contact opening
- 180sccm O_2, 50sccm SF_6,
  300mtorr, 150W
  120s for 300nm target etch depth

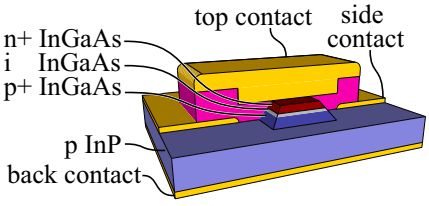


Figure C.2: Part two of the optimized fabrication flow for sub-micron sized diodes with separate contact pads.

i	0	1	2	3	4	5	6	7	8	9	
W_i[µm]	0	0.2	0.22	0.25	0.28	0.31	0.35	0.39	0.43	0.48	
i	10	11	12	13	14	15	16	17	18	19	
W_i[µm]	0.54	0.61	0.68	0.76	0.84	0.94	1.1	1.2	1.3	1.5	
i	20	21	22	23	24	25	26	27	28	29	
W_i[µm]	1.6	1.8	2	2.3	2.6	2.9	3.2	3.6	4	4.4	
i	30	31	32	33	34	35	36	37	38	39	40
W_i[µm]	5	5.5	6.2	6.9	7.7	8.6	9.6	11	12	13	15

Table C.1: The target widths W_i of the diodes and XSEM lines have an exponential distribution from W_1=200 nm to W_{40}=15 µm. W_i is the diameter of round-shaped diodes, the side length of square and diamond-shaped diodes and the width of the XSEM lines.

diamond shape (D) which is a square rotated by 45°, with the same side length W_i. There are 40 target dimensions 0.2 µm≤W_i≤15 µm with an exponential distribution, listed in table C.1 and plotted in figure C.4. These 3 shapes and 40 target dimensions (with names R01 to R40, D01 to D40 and S01 to S40) are repeated in 12 identical arrays as shown in figure C.3.

The second lithography level (labeled TOPCNT), is performed using i-line lithography.In this process step, sketched in figure C.2(i), we pattern contact pads on the top surface of the diode and on top of the adjacent BCB. Figure C.3) shows the contact pads consist of a 50×50µm^2 pad suited to land a probe tip, and a 26×26µm^2 pad which is connected with the diode. This way we avoid mechanically damaging the diodes due to direct contact with the probe tip.

The mask includes cross-section scanning electron microscopy (XSEM) lines L01 to L40 which have 3 mm target length and have the same target width as the diodes: W_i (figure C.4). These XSEM lines are only used to troubleshoot the fabrication flow. The mask also includes empty contact pads labeled R00, D00 and S00. These are used in electrical measurements at the end of the fabrication flow and have two purposes. First, we verify whether the BCB interlayer provides sufficient direct current (DC) isolation between the top contact and other two contacts. Second, we use these empty contact pads to measure the parasitic contact pad capacitance which is present in diode *C-V* measurements. We will characterize the pad capacitance in section 3.4.4.

We recommend defining the MESA level using e-beam lithography to preserve

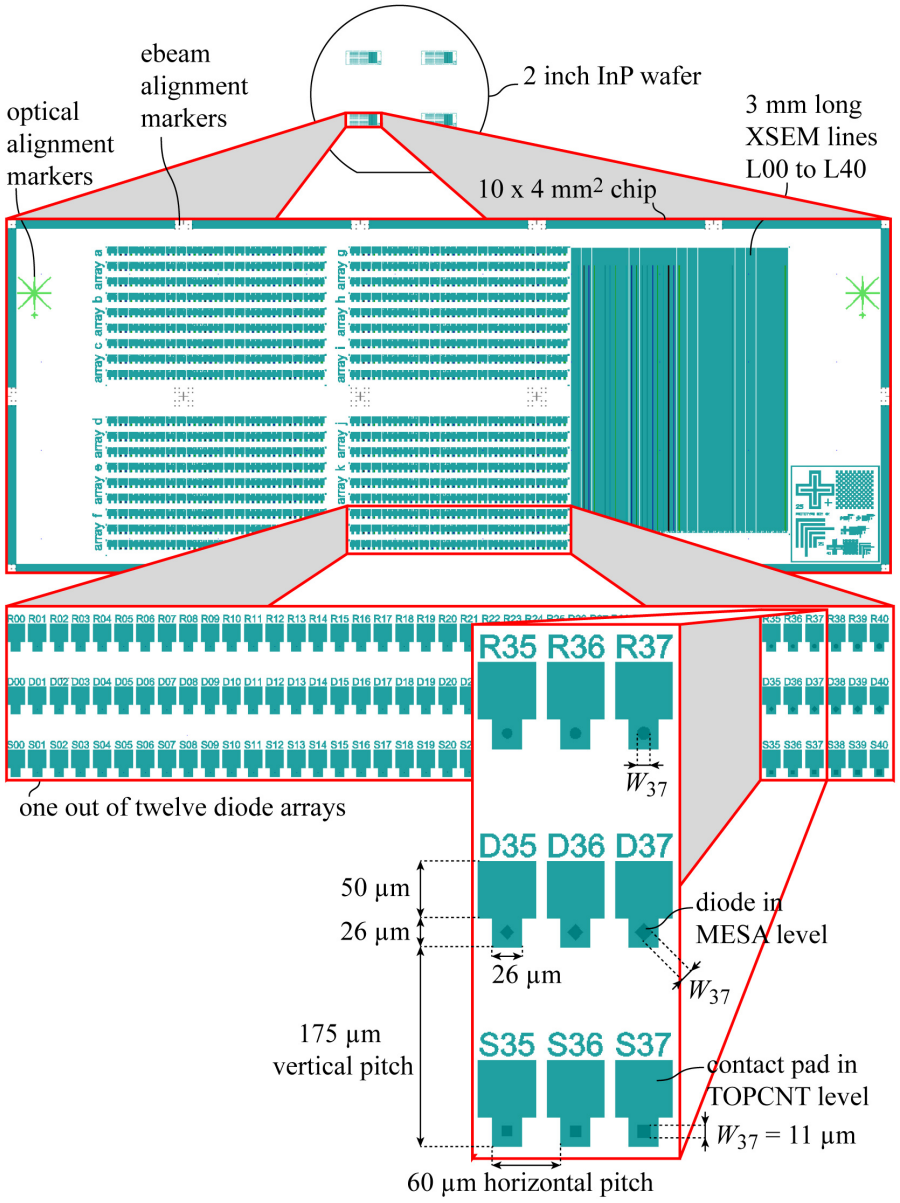


Figure C.3: The mask set designed for this fabrication flow, with three zoom levels. The shapes in dark green are the MESA level (bright field), and the shapes in light green are the TOPCNT level (bright field). The mask set also includes both levels in dark field mode, for lift-off processing.

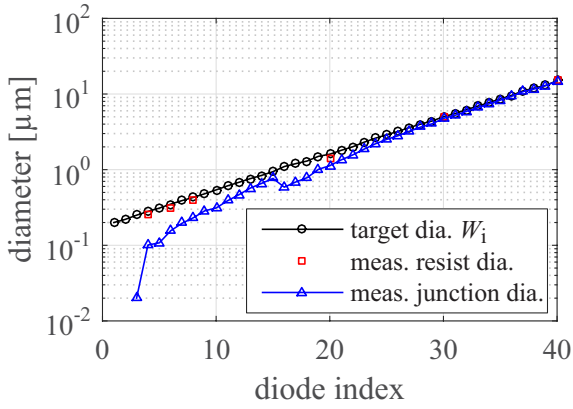


Figure C.4: The round diode target diameter Wi, the measured resist diameter measured using tilted SEM in figure C.5, and the measured junction diameter using top-view SEM as in figure C.8. Since the dose is abruptly lower for S16 compared to S15, the actual junction diameter of S16 is smaller than for S15.

the small dimensions, and defining the TOPCNT level using the much faster i-line lithography. However, the MESA level is also present on the glass mask for i-line lithography, and it can be used if only the large dimensions are required. On the glass mask, the MESA target dimensions W_{01} to W_{15} are modified to the minimum printable 1 µm.

The substrates are very valuable after MBE growth. Therefor, the MESA level of the entire $10{\times}4\,\mathrm{mm}^2$ chip is typically repeated four times, once on each quarter of a InP wafer, as shown in figure C.3. After development, the wafer is cleaved in four parts to make a split experiment with the same epitaxial growth but different mesa etching techniques or different contacting strategies. The pieces are labeled on the back side using a diamond pen to prevent accidental mix-up.

C.3 MBE epitaxial growth

The MBE growth is the first step of the process flow. It is schematically shown in figure C.1(a). All samples for $In_{0.53}Ga_{0.47}As$ homojunction diodes are grown on 2 inch InP wafers, which are doped p-type with Zinc with $N_A{=}5\times10^{17}\,\mathrm{cm}^{-3}$. All layer thicknesses and target doping concentrations for $In_{0.53}Ga_{0.47}As$ homojunction diodes are listed in figure 2.11 on p. 45.

The development of the MBE recipes is not the topic of this PhD, and we refer to the publication by Chu *et al.* for the growth of $In_{0.53}Ga_{0.47}As$ [116]. For the growth of $GaAs_{0.5}Sb_{0.5}/In_{0.53}Ga_{0.47}As$ heterojunctions, we refer to the publication by El Kazzi *et al.* [106].

C.4 Hard mask patterning: option 1

The process step of patterning the SiO_2 hard mask is shown in figure C.1(b). The most straightforward solution in the imec III-V lab is to use a combination of resist patterning and pattern transfer using Buffered HF (BHF). However, the lateral SiO_2 wet etching would lead to hundreds of nanometers of undercut resist, and a resulting uncontrolled diode mesa dimension. Therefore, this process step has to be developed from scratch, resulting in two different approaches.

The first approach consists of depositing a hard mask on the samples (section C.4.1), patterning a layer of resist using e-beam lithography (section C.4.2), transferring this pattern to the hard mask using dry etching, and removing the remaining resist (both in section C.4.3). It is discussed below in more detail. Of all processing steps in this appendix, the development of this step was the most complicated, mainly due to the creation of etch by-products (polymers) during dry etching, which are difficult to remove. All $In_{0.53}Ga_{0.47}As$ diodes in chapter 3 are fabricated using this first option.

The second option was developed at a later time and consists of only a single step: patterning a layer of Flowable Oxide (FOx) using e-beam lithography, which immediately serves as the SiO_2 hard mask. It is further discussed in section C.5. All $In_{0.53}Ga_{0.47}As/GaAs_{0.5}Sb_{0.5}$ diodes in chapter4 use this much faster second option.

C.4.1 Hard mask selection

First we select the correct hard mask material suitable for pattern transfer using dry etching. Compared to metals, SiO_2 is preferred as hard mask, because it is inert to the acid-peroxide wet etching solutions used for the III-V materials. The most commonly used types of SiO_2 in the imec III-V lab are deposited using Chemical Vapor Deposition (CVD) or Physical Vapor deposition (PVD) and are:

- SiO_2 deposited using CVD at T=350°C with a *Oxford Plasmalab 100-ICP 380* at a pressure p=3.4 mtorr and a deposition rate of 9 nm/min. We will call this the 'CVD 350°C SiO_2'

	before etch		after etch		
hard mask	R_q [nm]	R_p [nm]	etch rate	R_q [nm]	R_p [nm]
CVD SiO_2 at 150°C	0.4	1.4	56 nm/min	0.7	1.8
CVD SiO_2 at 350°C	0.4	1.0	61 nm/min	0.3	0.9
PVD SiO_2	0.4	1.1	8.3 nm/min	1.8	3.5

Table C.2: 300 nm of each material are deposited. The RIE recipe is 50 cm^3/min CHF_3 and 25 cm^3/min CF_4, P=150 W and p=100 mtorr. The roughness and etch rate are measured with a profilometer tool.

- SiO_2 deposited using CVD at T=150°C. We will call this the 'CVD 150°C SiO_2'
- SiO_2 deposited by PVD (sputtering), with a *Pfeiffer Spider 630*. We will call this the 'PVD SiO_2'

A first factor which influences our hard mask selection is the SiO_2 dry etch speed. It must be sufficiently high compared to the resist dry etch speed, in order etch the full SiO_2 layer. The SiO_2 dry etch speed is tested using Reactive Ion Etching (RIE) in a *ML200RF* tool. The dry etch recipe used for this etch speed test and the results are shown in table C.2. Similar etch speeds are observed for the CVD 150°C SiO_2 at (56 nm/min) and the CVD 350°C SiO_2 (61 nm/min), but there is a significantly lower etch speed for PVD SiO_2 (8.3 nm/min) .

The second factor impacting our hard mask selection is the roughness after deposition and after dry etch, which must be as low as possible. After deposition, the root mean square roughness R_q and maximum peak height roughness R_p are shown in Table C.2 and are comparable for the three oxides ($R_p \approx 1$ nm). However, after etch the roughness of the PVD SiO_2 increases to R_p=3.5 nm. Due to this increased roughening during dry etch, and the low etch rate compared to the resist dry etch rate discussed in the previous paragraph, the PVD SiO_2 cannot be used as a hard mask.

The last factor is the presence of voids or impurities in the hard mask. After dry etching of the different hard masks, residues are seen using SEM for the CVD 150°C SiO_2, shown in figure C.10(a) on p. 200. Little to no residues are seen for CVD 350°C SiO_2, as shown in figure C.10(b-l). Therefore, the latter is chosen as hard mask material.

C.4.2 Resist patterning

For the e-beam lithography of the MESA mask level, we choose the resist series ma-N 2400 from *Micro Resist Technology* [144] because it is a negative tone resist. This results in faster e-beam write time, because only the small mesa surfaces need to be exposed (less than 0.4% of the chip surface). If we use a positive resist like Poly-Methyl Methacrylate (PMMA), we need to expose a much larger surface (99.6%). Furthermore, ma-N 2400 resists have a high resistance to dry etching compared to other resists [144]. From the family of ma-N 2400 resists, the ma-N 2405 or ma-N 2403 are equivalent and either one can be used for this fabrication step. Although the former is suited for thicker resist layers, the spinning speeds are chosen to obtain a ≈300 nm thick resist layer in both cases.

The process steps are as follows:

- Resist spinning of ma-N 2405 or ma-N 2403. Ma-N 2405 is spun at 6000 rpm for 60 s, resulting in a thickness of 340 nm. Ma-N 2403 if spun at 2000 rpm for 30 s, resulting in a thickness of 280nm.
- Resist bake in oven at 110°C for 30 min
- E-beam exposure: features with $200\,\text{nm} \leq W_\text{i} \leq 1\,\mu\text{m}$ get a dose of $200\,\mu\text{C}\,\text{cm}^{-2}$. Features with $1\,\mu\text{m} < W_\text{i} \leq 15\,\mu\text{m}$ get a dose of $60\,\mu\text{C}\,\text{cm}^{-2}$
- develop for 150 s in ma-D 525, a metal-ion-free inorganic alkaline developer ordered from the company *Micro Resist Technology*
- Water rinse

Figure C.5 shows the patterned ma-N 2405 resist on the SiO_2 layer (CVD 350°C). The diameters of the ma-N 2405 shapes are close to the target diameters on the mask, as shown in figure C.4, especially for the larger R30 to R40.

The higher e-beam dose for sub-micron features (like S01-S15) compared to super-micron features (like S16-S40) is the result of numerous dose tests. However, since the devices are placed in two dose groups, there is an abrupt dose change between S15 and S16. This causes S16 to be relatively under-exposed, and therefore its measured junction diameter is smaller than for S15 (figure C.4), even though the target diameter is larger. This minor inconvenience is solved when using the alternate processing step in section C.5, where each diode has its own unique dose, and the abrupt dose change is avoided.

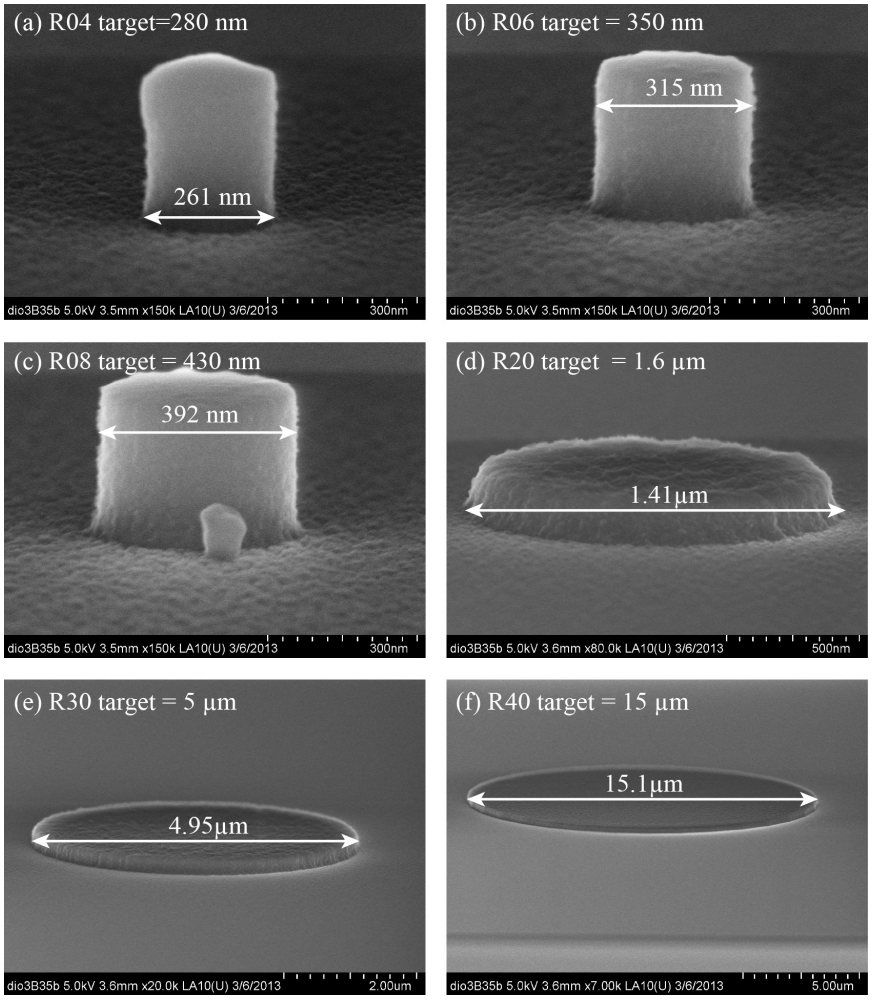


Figure C.5: These tilted SEM images show e-beam patterned ma-N 2405 resist (round shapes) on top the SiO_2 hard mask (CVD 350°C). For the largest shapes R30 and R40, the measured shape diameters are close to the target diameters.

C.4.3 Hard mask dry etch and resist strip

The pattern in the e-beam resist then needs to be transferred to the underlying SiO_2 hard mask by dry etching. The resist and any redeposited polymer residues must then be stripped. Using the available gases in the *ML200RF* RIE tool (CF_4, CHF_3, SF_6, N_2, O_2), and after many discussions with the imec etch experts, two possible strategies are established to develop this process step.

In the first approach, polymerization is avoided in first place by using a SiO_2 dry etching recipe with a higher amount of fluorine, or by adding a small amount of O_2. The recipes and corresponding XSEM images are shown in figure C.6.

- Recipe (a) consists of pure CF_4, which is the least polymerizing according to internal discussions with imec etch experts. However, it also has a relatively fast resist etch rate (bad selectivity), leading to the sloped SiO_2 sidewall seen at the edge of figure C.6(a).

- In recipes (b), (c) and (d), SiO_2 is etched with a mix of CF_4 and CHF_3 with different ratios. In a second step, the remaining resist is etched using an O_2 plasma. Nevertheless, sidewall polymers are visible for the three etch recipes. Additionally, un-etched nanowire-like protrusions are visible adjacent to the hard mask lines. These are created due to un-etched particles which result in micromasking. The origin of these particles is unknown.

- Recipe (e) is a mix of pure CHF_3 with O_2 to reduce polymerization. However, polymers are still present, and many particles are visible adjacent to the lines.

In the second approach, polymerization is tolerated during the SiO_2 etch. This allows the use of pure CHF_3 which etches SiO_2 with a higher selectivity compared to the e-beam resist. The recipes focus on removing the polymers after dry etching the SiO_2. Corresponding XSEM images are shown in figure C.6.

- Recipe (f) uses pure CHF_3 in six steps of 30 s, with a N_2 purge between each step to prevent overheating of the resist during dry etch. No particles are visible adjacent to the hard mask lines, but thick polymer layers are deposited on the sidewalls of the remaining resist and SiO_2. The sidewalls of the SiO_2 are sloped due to polymer formation during dry etching.

- In recipe (g), we start with the same etch conditions as (f). The polymers are removed successfully using a BHF dip. However, the dimensions of the SiO_2 are uncontrolled due to the lateral etching, the sidewalls are very rough and on some lines crystals nucleate. The composition of these crystals is not investigated.

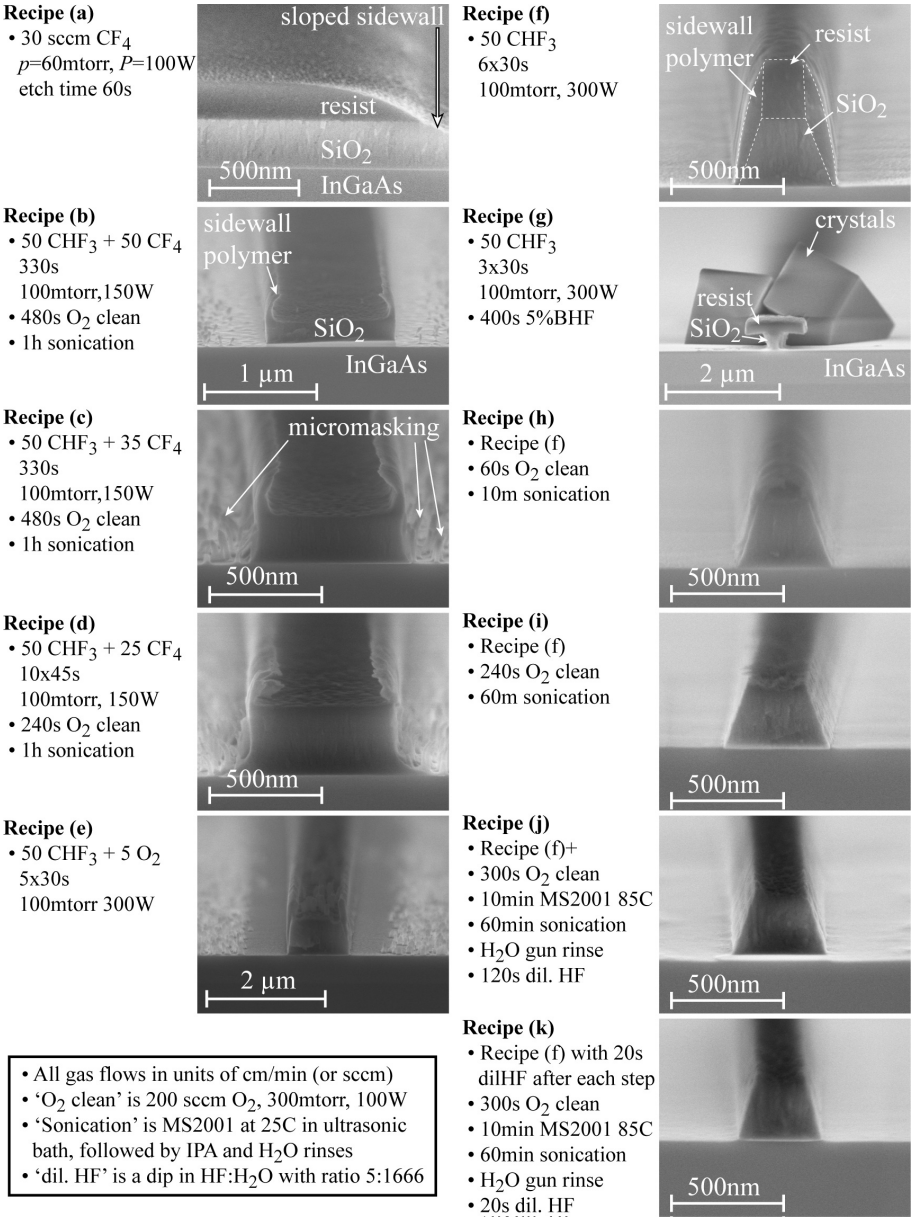


Figure C.6: All hard mask dry etching recipes are tested using a dedicated e-beam mask with XSEM lines with widths 100, 200, 500 and 1000 nm. All dry etching is done in the *ML200RF* RIE tool, in chamber #2 for recipes (a)-(i) and chamber #1 for recipes (j)-(k). Recipes (d)-(k) are divided in multiple dry etch steps with a N_2 purge between each step to prevent resist overheating during dry etch. Microstrip MS2001 is a solvent, and IPA is isopropylacohol.

- For recipes (h) and (i), we also start with the same etch conditions as (f). After dry etching, a O_2 plasma clean is performed for 60 s or 240 s for recipes (h) and (i), respectively. The latter results in a complete removal of the sidewall polymers. However, this recipe is not fully stable. Depending on previous users who used the tool or other unknown factors, there are sometimes particles present after dry etching. Recipes (a) to (i) are all performed in the *ML200RF* RIE tool, and more specifically in the heavily used chamber #2 of the tool.

- Recipe (j) adds a few improvements to recipe (i) which lead to a fully stable recipe. The dry etch is performed in chamber #1 of the *ML200RF* RIE tool. For this chamber the amount of users is very limited, and no metals are allowed. Furthermore, the O_2 plasma clean is slightly longer, there is an additional 10 min clean in microstrip MS2001 at 85°C, and a 60 min sonication in MS2001 is added. The sample is rinsed by spraying water using the water gun. Finally, the sample is dipped in a diluted HF solution ($HF:H_2O$ with volumetric ratio 5:1666) for 120 s, and it is rinsed in a water overflow bath and dried with a N_2 gun.

- Recipe (k) adds an additional improvement to recipe (j). After each of the six SiO_2 dry etch steps, the sample is unloaded from the tool and a 20 s diluted HF dip and water rinse is performed every time.

Overall, recipes (j) and (k) in figure C.6 lead to the most stable and clean SiO_2 dry etch and resist strip. Therefore these recipes are used for the fabrication of all $In_{0.53}Ga_{0.47}As$ diodes discussed in chapter 3.

C.5 Hard mask patterning: option 2

Because the hard mask patterning processes described in section C.4 are very time-consuming, an alternative, much simpler recipe is developed for the fabrication of $In_{0.53}Ga_{0.47}As/GaAs_{0.5}Sb_{0.5}$ Esaki diodes. The negative tone e-beam resist FOx12 is patterned and immediately used as a hard mask. FOx12 is Flowable Oxide (FOx) from the company *DOW Corning*. It is a liquid solution of the inorganic polymer Hydrogen silsesquioxane (HSQ) [145], and consists mainly of SiO_2 after e-beam. The process steps are the following:

- FOx12 is spun at 900 rpm for 60s, to obtain a FOX12 thickness of 175 nm after bake.

- It is baked in an oven at 90°C for 40 min.

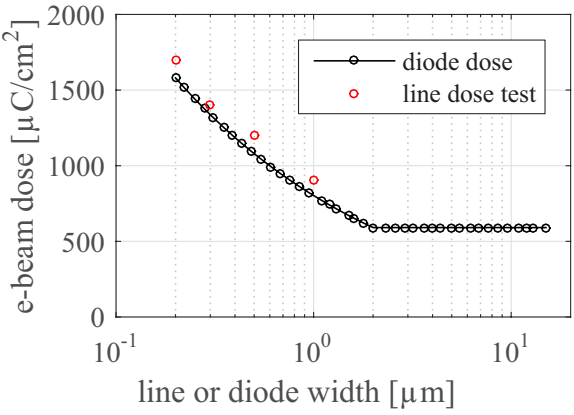


Figure C.7: Using a e-beam dose test on FOx12 lines, we establish the applied dose for every diode size. Since the diodes are round, square or diamond shaped, their dose is taken slightly smaller than for long lines.

- The MESA level is exposed by e-beam. Each diode is exposed with a dose that depends on its dimension W_i. The doses are shown in figure C.7. Since these lines have a more extended geometry than the diodes, the doses for the latter are chosen $100\,\mu\mathrm{C\,cm^{-2}}$ lower than the doses for the lines.
- The FOx12 is developed in *Silicon etch* (25% Tetramethylammoniumhydroxide or TMAH) for 60 s
- The samples are dipped in the TMAH solution OPD262:H_2O 1:10 for 10 s, rinsed in the overflow bath for 2 min, and dried with the N_2 gun.

C.6 Back contact deposition

The 'back contact' deposition on the InP substrate (step (c) in figure C.1) is optional. It is not required if a 'side contact' is planned (step (e) in figure C.1). Two different recipes are available for the back contact deposition. All samples in this thesis are processed using the first recipe, because the second recipe was established later.

In the first recipe, 30 nm of the alloy AuZn is evaporated on the backside, followed by the evaporation of 70 nm Au. This metal stack requires an anneal of

5 min at 400°C. Due to this anneal, this process step must be performed before the BCB interlayer deposition (step (f) in figure C.2), which does not tolerate this high anneal temperature. The recipe is as follows:

- The photoresist IX845 is spun and baked on the front side of the sample, to prevent damage.
- 30 nm AuZn and 70 nm Au are evaporated on the back side.
- The protective resist is removed from the front side using acetone from a spray bottle. The sample is rinsed in IPA and dried with a N_2 gun.
- The sample is placed on a silicon carrier wafer in the *p-alloy oven* tool, and annealed at 400°C for 5 min in N_2 ambient. The back contact color then changes from gold to pink.

The alternative, second recipe consists of sputtering Molybdenum and Aluminum on the back side using the *Pfeiffer spider 630* sputtering tool. Since this contact does not require annealing, it is ideally done at the end of the flow, after step (j) in figure C.2.

C.7 Diode wet etching

The semiconductor wet etching step (shown schematically in figure C.1(d)), is developed for $In_{0.53}Ga_{0.47}As$ with the following criteria in mind. First, the wet etch recipe may not affect the SiO_2 hard mask. Second, the $In_{0.53}Ga_{0.47}As$ roughness on the exposed sidewall planes must be as low as possible. Anisotropic wet etching is preferable to obtain nearly atomically flat sidewall surfaces.

The following commonly used $In_{0.53}Ga_{0.47}As$ wet etch solutions are selected.

- x parts citric acid solution, x parts peroxide solution and y parts water. The citric acid solution is 1 gram citric acid monohydrate diluted in 1 ml de-ionized water. The peroxide solution is the industry standard 30 % H_2O_2 and 70 % de-ionized water.
- x parts sulfuric acid, $3x$ peroxide solution and y parts water. The sulfuric acid has nearly 100% concentration.

The etch speed of both solutions is calibrated for different volumetric ratios x and y. The calibration is done by patterning lines of 10 nm Ti/100 nm Au on a $In_{0.53}Ga_{0.47}As$ sample. The step height of the metal line is then measured using the *Dektak profilometer* tool. The samples are etched in the different solutions, and the step height is measured again. The resulting $In_{0.53}Ga_{0.47}As$ etch rates

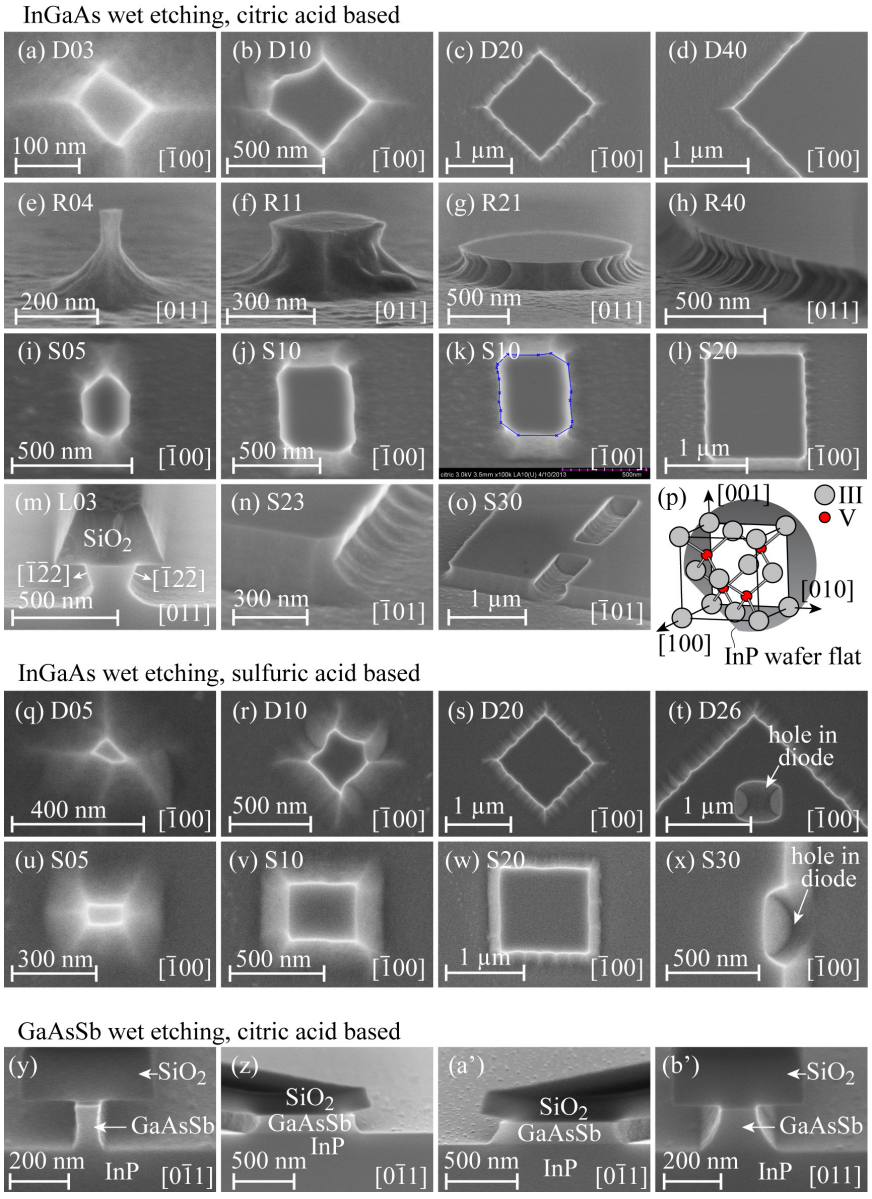


Figure C.8: All images show $In_{0.53}Ga_{0.47}As$ only, unless otherwise labeled. The SEM viewing direction is indicated at the bottom of each image. All top-view images (in the [$\bar{1}$00] direction) have the wafer flat oriented towards the bottom of the image. (k) shows an example of the top area extraction using the program *Engauge.exe*. (p) shows the wafer orientation according to the wafer supplier specifications sheet: the wafer surface orientation is (100) and the primary flat is (0$\bar{1}\bar{1}$). The images in (o), (t) and (x) had unexpected holes in the hard mask, leading to additional sidewall surfaces.

are shown in table C.3 for the citric acid based solution and table C.4 for the sulfuric acid based solution. For these respective solutions, the volumetric ratios 1:1:320 and 1:3:1000 appear to give the smoothest $In_{0.53}Ga_{0.47}As$ surface after etch (SEM images not shown), and give a good compromise between sufficiently fast but controllable etch speed, so these solutions are chosen for the processing of all diode samples.

Volumetric ratio $x : x : y$	1:1:1600	1:1:320	1:1:160	1:1:50	1:1:0
Etch rate [nm/min]	1.62	7.2	11.4	35.4	86

Table C.3: $In_{0.53}Ga_{0.47}As$ etch rate in x parts citric acid solution, x parts standard peroxide solution and y parts water with different volumetric ratios $x : x : y$. The citric acid solution is 1 gram citric acid monohydrate diluted in 1 ml de-ionized water. The standard peroxide solution is 30 % H_2O_2 and 70 % de-ionized water. The molarity of the $x : x : y$=1 : 1 : 0 solution is 1.58 M.

Volumetric ratio $x : 3x : y$	1:3:1000	1:3:160
Etch rate [nm/min]	22.8	90

Table C.4: $In_{0.53}Ga_{0.47}As$ etch rate in x parts sulfuric acid, $3x$ standard peroxide solution and y parts water with different volumetric ratios $x : 3x : y$. The acid molarity of the 1 : 3 : 160 solution is 0.11 M.

Figure C.8 shows SEM and XSEM images of a $In_{0.53}Ga_{0.47}As$ test sample after wet etching using the SiO_2 hard mask, and subsequent removal the hard mask using a BHF dip to expose the mesa structures. The test sample is included in the fabrication split, together with the $In_{0.53}Ga_{0.47}As$ diodes for BTBT calibration in chapter 3. Except for the BHF dip, it received the same processing steps, and its mesa geometries are representative for all other $In_{0.53}Ga_{0.47}As$ diodes.

Wet etching of $In_{0.53}Ga_{0.47}As$ with citric acid based solution gives a re-entrant sidewalls for square diodes, because the etch speed is lowest for the $(\bar{1}\ 2\ \bar{2})$ and $(\bar{1}\ \bar{2}\ 2)$ planes, shown at the left and right sides of figure C.8 (m). XSEM images of the etched diode mesa further in the fabrication flow (figure C.11(b)) show the same re-entrant slopes. The other sidewalls of the square shaped diodes also appear to be smoother (top and bottom sides of figures C.8 (i) to (l)). We therefore expect that the square shapes will give the lowest sidewall defect concentration, compared to the round or diamond mesa shapes. From electrical results, we confirm that round diodes have the highest sidewall defect concentration, but comparison between square and diamond shapes give inconsistent results (not shown).

For wet etching of $In_{0.53}Ga_{0.47}As$ with the sulfuric acid based solution, we observe smoother sidewalls for square shaped diodes (figures C.8 (u-x) than diamond shaped diodes (figures C.8 (q-t). Although a sidewall defect current comparison between sulfuric based and citric based etched diodes would be interesting, we have no electrical results from the sulfuric acid based diodes. Further in the fabrication flow, shorts circuits occurred between the top contact and side contact in several samples (as shown in figure C.13(b)), and no samples with sulfuric based etching have usable electrical results. However, in section 3.3 we observe an acceptably low sidewall defect current for citric acid etched diodes.

The wet etching recipes are not re-optimized for $GaAs_{0.5}Sb_{0.5}$. Instead, the citric acid-based 1:1:320 solution is applied to both these materials. Figure C.8(y) to (b‘) shows the $GaAs_{0.5}Sb_{0.5}$ wet etched sidewalls, with the XSEM image taken in different directions. The wet etch is anisotropic, but with a lower selectivity along the different directions compared to $In_{0.53}Ga_{0.47}As$.

C.8 Junction area measurement

In section 3.3.4, we will normalize the measured BTBT current with respect to the tunnel junction area. Therefore, the junction areas are measured using top-SEM for all diodes R01-R40, D01-D40, S01-S40 for the citric acid based etching. The tunneling junction area is not identical to the easily measured exposed top surface (shown in figure C.8(k) by the blue line), because the tunneling junction is located 40-90 nm below the surface.

Therefore, the junction area is measured according to the following procedure: For the diamond shapes (D), we estimate that the tunneling junction is undercut by 20 nm compared to the top surface, and this in all four directions. For the square shapes (S), we measure 72° re-entrant sidewalls at the left and right sides seen in figure C.8(m) and tapered sidewalls along top and bottom sides, seen in figure C.8(k). For the round shapes (R), 20 nm undercut is assumed for the left and right sides seen in figure C.8(g) and no undercut is assumed for the front and back sides in the same figure.

For R01-R40, the resulting junction area is converted to a average junction diameter and shown in figure C.4. The measured junction diameter is significantly smaller than the measured resist diameter due to the undercut hard mask, and the re-entrant sidewall slopes, which are both seen clearly in figure C.8(m). Due to the estimated values for the undercut, and the more irregular shapes for the smallest diodes, the procedure for the junction area extraction is less accurate for the smallest diodes than for the largest diodes. This difference will be further discussed in section 3.3.4. Another observation

in figure C.4 is the larger junction diameter for R15 compared to R16. This is due to the sudden change of e-beam dose between those two dimensions, and is discussed in section C.4.2.

C.9 Side contact deposition

The side contact deposition to p-$In_{0.53}Ga_{0.47}As$ is shown schematically in figure C.1(e). For the choice of metals, the combination Ti/Pt/Au is often chosen for n-type and p-type $In_{0.53}Ga_{0.47}As$ according to reference [146]. However, with this stack the Fermi level at the metal-semiconductor interface pins near the conduction band edge. For a contact to n-$In_{0.53}Ga_{0.47}As$, the tunneling barrier height is nearly zero, but for p-$In_{0.53}Ga_{0.47}As$, it is nearly the whole bandgap. Therefore, for p-$In_{0.53}Ga_{0.47}As$ a low specific contact resistance $R_c < 1 \times 10^{-7}\,\Omega\,cm^2$ can only be achieved with high p-type doping $N_A > 1 \times 10^{20}\,cm^{-3}$.

The stack Pd/Ti/Pt/Au yields better performance for p-$In_{0.53}Ga_{0.47}As$ due to a better band alignment. The workfunction of Pd (5.12 eV) is higher than for Ti (4.33 eV) [146], which aligns better to the valence band of $In_{0.53}Ga_{0.47}As$ (5.24 eV from the vacuum level). Using this stack, values of $R_c = 6 \times 10^{-5}\,\Omega\,cm^2$ and $6 \times 10^{-6}\,\Omega\,cm^2$ have been reported for doping concentrations $N_A = 1 \times 10^{19}\,cm^{-3}$ and $2 \times 10^{19}\,cm^{-3}$ [146] .

Therefore, we have deposited the following stack with the *VG* metal evaporation tool: 3 nm Pd/3 nm Ti/20 nm Pd/30 nm Au/5 nm Ti. The first layer of Pd is used to have a better band alignment for p-$In_{0.53}Ga_{0.47}As$. The second layer of Ti acts has an native oxide gettering mechanism. The third layer (Pd) acts as a diffusion barrier [146, 147]. The Au layer lowers the metal sheet resistance, and the final Ti layer provides a reactive top surface with dangling bonds to have a good adhesion of the BCB interlayer [148], which is deposited in the following process step. This metal stack is used for all $In_{0.53}Ga_{0.47}As$ diodes with a side contact. Figures C.9(a) and (b) show XSEM and tilted XSEM views of a similar side contact. It is deposited self-aligned with the *VG* tool and does not contaminate the diode sidewalls.

However, the *VG* tool is now disassembled. A first possible alternative is Mo/Al sputtering with the *Pfeiffer spider 630* tool. XSEM inspection (figure C.9(c)) shows no visible metal contamination on the sidewall. Mo/Al sputtering using the *LAB18* tool is also investigated, but this deposition is more conformal and metal contamination on the sidewall is visible (figure C.9(d)). A specific contact resistance of $R_{c,p} = 1.75 \times 10^{-4}\,\Omega\,cm^2$ for Mo/Al to p-$In_{0.53}Ga_{0.47}As$ is measured using TLM measurements and the following recipe.

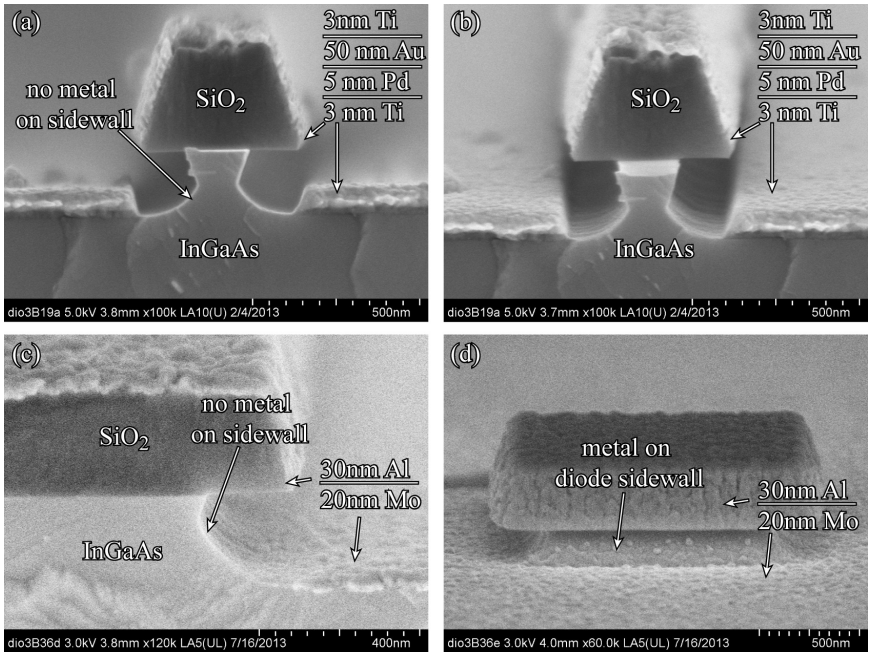


Figure C.9: (a) and (b) show XSEM image at two different angles of a diode with 3nm Ti/5nm Pd/50nm Au/5nm Ti. (c) and (d) have Mo/Al as side contact sputtered with the *LAB18* and *Pfeiffer spider 630* tools, respectively.

- On a p-$In_{0.53}Ga_{0.47}As$ sample with $N_A = 2 \times 10^{19}\,cm^{-3}$, the resist IX845 is spun and baked. A TLM pad pattern is exposed and developed.
- The sample is dipped in a solution 1:5 $HCl:H_2O$ for 30 s to remove the native oxide, and immediately put in *Pfeiffer spider 630* load lock.
- 20 nm Mo/30 nm Al is sputtered on the sample.
- The excess metal is lifted using hot microstrip MS2001

C.10 BCB spinning and curing

The planarization step with the BCB interlayer (shown schematically in figure C.2(f)) is done according to the BCB specifications sheet in reference [149]. The details are as follows.

- spinning of BCB3022-46 at 3000 rpm for 60 s. This results in a thickness of 2.9±0.1µm after a full cure.
- The sample is transferred to a vacuum oven with programmable temperature profile (*VAC oven* tool) as fast as possible.
- 15 minute ramp to 100°C in the oven
- 15 minute soak at 100°C
- 15 minute ramp to 150°C
- 15 minute soak at 150°C
- 60 minute ramp to 250°C
- 60 minute soak at 250°C to achieve full cure
- cool to room temperature

C.11 BCB recess

The 2.9 µm thick BCB layer is then recessed to ≈300 nm (figure C.2(g)), until the hard mask covered with the side contact metal is revealed. This is done by dry etching in the *ML200RF* RIE tool. The recipe is taken from the BCB specifications sheet [149]: 180 cm^3/min O_2, 50 cm^3/min SF_6, 300 mtorr and 150W. The BCB recess rate of this recipe is quite fast and unstable. Over several samples, we measure 700±40 nm/min.

After recess, the BCB must be thinner than the combined thickness of the diode mesa height and the hard mask thickness (typically 150 nm + 300 nm) to allow top contact opening. This corresponds to a BCB recess of at least 2.45 µm. The BCB must be thicker than the peak roughness of the underlying p-$In_{0.53}Ga_{0.47}As$ and optional side contact (not measured) to prevent a short circuit. However, using electrical measurements at the end of the fabrication flow, we observe that if the recessed BCB is thinner than 250 nm, a short circuit is created between the top contact and the side contact. The exact reason for these shorts is uncertain, but figure C.13(b) possibly shows a parasitic electrical connection between the top and side contacts.

Due to the unstable etch rate and the narrow margins (minimum 2.45 µm and maximum 2.65 µm recess depth) most failures happen at this process step, and are due to over-recessing the BCB. Therefore, the recess is done in multiple steps, and the remaining BCB thickness is verified after each recess step. This is done

by scratching away part of the relatively soft BCB with tweezers, exposing the underlying p-$In_{0.53}Ga_{0.47}As$ with optional side contact. The BCB thickness is then measured using the *Dektak* profilometer tool. Alternatively, the remaining BCB thickness can be measured using the *thin film measurement* reflectometer tool. After each recess step, we also measure if the hard mask is exposed by scanning the profile over the diode hard mask with *Dektak* profilometer tool. If an abrupt step is detected, the hard mask is exposed and sufficient BCB has been etched.

C.12 Top contact opening

The top contact is then opened as shown schematically in figure C.2(h). If the side contact metal stack Pd/Ti/Pd/Au/Ti is present on the hard mask, it is first removed with a (home-built) *Xenon ion miller* tool. The standard ion milling recipe is used for 30 cycles of 30 s, with 60 s of cooling between each cycle. If a metal stack Mo/Al is present on the hard mask, it is removed using TMAH-based wet etching of Aluminum, and H_2O_2 wet etching of Molybdenum. The SiO_2 hard mask is then wet etched using a BHF dip for 30 s.

Figure C.10(a) shows a tilted SEM image of the opened top contact, but residues are present in the contact hole because the SiO_2 hard mask is deposited using a different tool for this test sample. Figures C.10(a) to (k) show the opened top contact with tilted view SEM, and almost no residues are present with the CVD 350°C SiO_2. The shape of the exposed top $In_{0.53}Ga_{0.47}As$ surfaces are identical as in figure C.8.

C.13 Top contact deposition and patterning

The top contact is then deposited on the exposed n-$In_{0.53}Ga_{0.47}As$ surface and patterned as shown in figure C.2(i). Either Mo/Au or Mo/Al are chosen as top contact metal, and both are deposited with the *Pfeiffer spider 630* sputtering tool. Figure C.11 shows the metal in contact with the top n-$In_{0.53}Ga_{0.47}As$ region. TLM measurements of 10 nm Mo/30 nm Au on a blanket layer of n-$In_{0.53}Ga_{0.47}As$ result in R_c=$8.8 \times 10^{-6}\,\Omega\,cm^2$.

In order to pattern the metal into contact pads, optical lithography is chosen instead of e-beam lithography due to the faster processing. Several patterning recipes are explored, and only the last two recipes are successful.

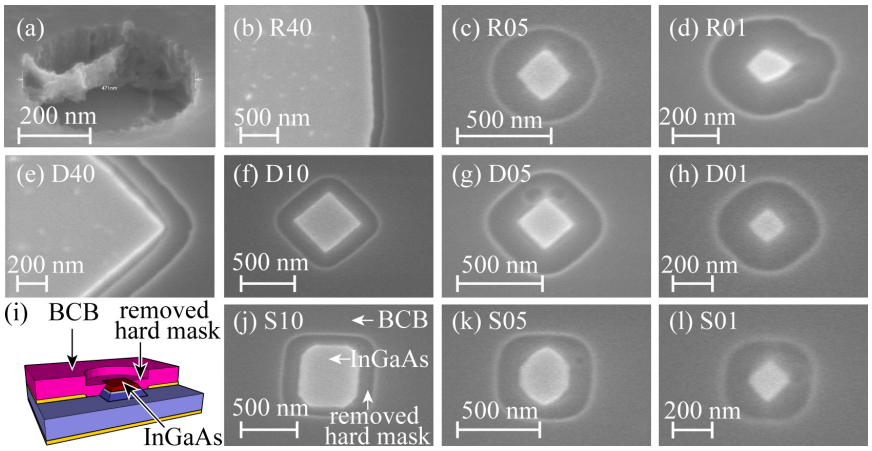


Figure C.10: All SEM images in this figure are top views of the diode with (i) the SiO_2 hard mask removed to reveal the n-$In_{0.53}Ga_{0.47}As$ surface. (a) After removal of the CVD 150°C SiO_2 hard mask in 90 s BHF, residues are still present. (b-h,j-l) Using CVD 350°C SiO_2, little to no residues are present after removal of the SiO_2 hard mask.

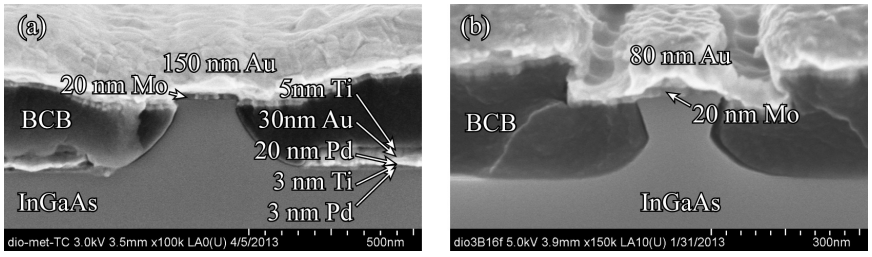


Figure C.11: (a) A sulfuric acid based etched mesa with side contact and top contact. (b) A citric acid based etched mesa with top contact but without side contact. Delamination of the $In_{0.53}Ga_{0.47}As$/BCB interface is observed on the right side of the diode, but this is a result of wafer cleaving and electron bombardment during the XSEM inspection.

The first unsuccessful recipe consists of patterning using liftoff. A LOR1A/IX845 bilayer stack is deposited on the BCB and patterned using the TOPCNT level (dark field) of the mask. Mo/Au is then sputtered and lifted for 12 hours in either microstrip MS2001, or acetone at 50°C, or TMAH-based developer OPD5262. The results are shown in the respective figures C.12(a), (b) and (c). The microscope images show cracking of the BCB layer, delamination at the BCB/$In_{0.53}Ga_{0.47}As$ interface and the BCB/metal interface.

The second unsuccessful recipe consists of patterning using ion milling, and resist removal using acetone or oxygen plasma. The Mo/Au contact is first sputtered on the exposed n-$In_{0.53}Ga_{0.47}As$ and BCB. A LOR1A/IX8245 bilayer stack is then deposited on the metal stack and patterned using the TOPCNT level (bright field) of the mask. The metal is then ion milled in the *Xe Ion miller* tool for 25 cycles of 30 s, and 60 s cooling between each cycle. The intermediate result in figure C.12(d) shows well-defined contact pads. However, these pads are still covered by the bilayer resist stack with an additional hardened crust due to the ion milling. After 1 hour of resist removal in acetone at 50°C, the crust is still partially present (figure C.12(e)). Subsequent RIE with the *ML200RF* RIE tool (5 cycles of 60 s, 180 cm^3/min O_2, 50 cm^3/min SF_6, 300mtorr, 150W) did remove the exposed BCB adjacent to the contact pads, but did not remove the hardened crust (figure C.12(f)).

The first successful recipe is similar to the previous recipe. The resist is not removed using acetone but with a treatment of 10 min microstrip MS2001 at 85°C, followed by 10 min of sonication in the same MS2001. The sample is then rinsed using IPA, and by spraying water with the H_2O showerhead for 2 min. All diode electrical results discussed in this thesis use this recipe for top contact patterning.

The second successful option is patterning using wet etching of the top contact metal stack. After sputtering of Mo/Al using the *Pfeiffer spider 630* sputtering tool, IX845 is deposited on the metal stack and patterned using the TOPCNT level (bright field) of the mask. The Aluminum is then wet etched using OPD5262, the sample is rinsed in water, the Molybdenum is wet etched in H_2O_2 and the sample is rinsed in water again. Both metals are etched until the metal is no longer visible by eye. This second recipe is faster than the first one and is therefore recommended for future diode fabrication.

C.14 Side contact opening

The last step of the fabrication flow is the opening of the side contact by recessing the exposed BCB adjacent to the contact pads, as shown schematically

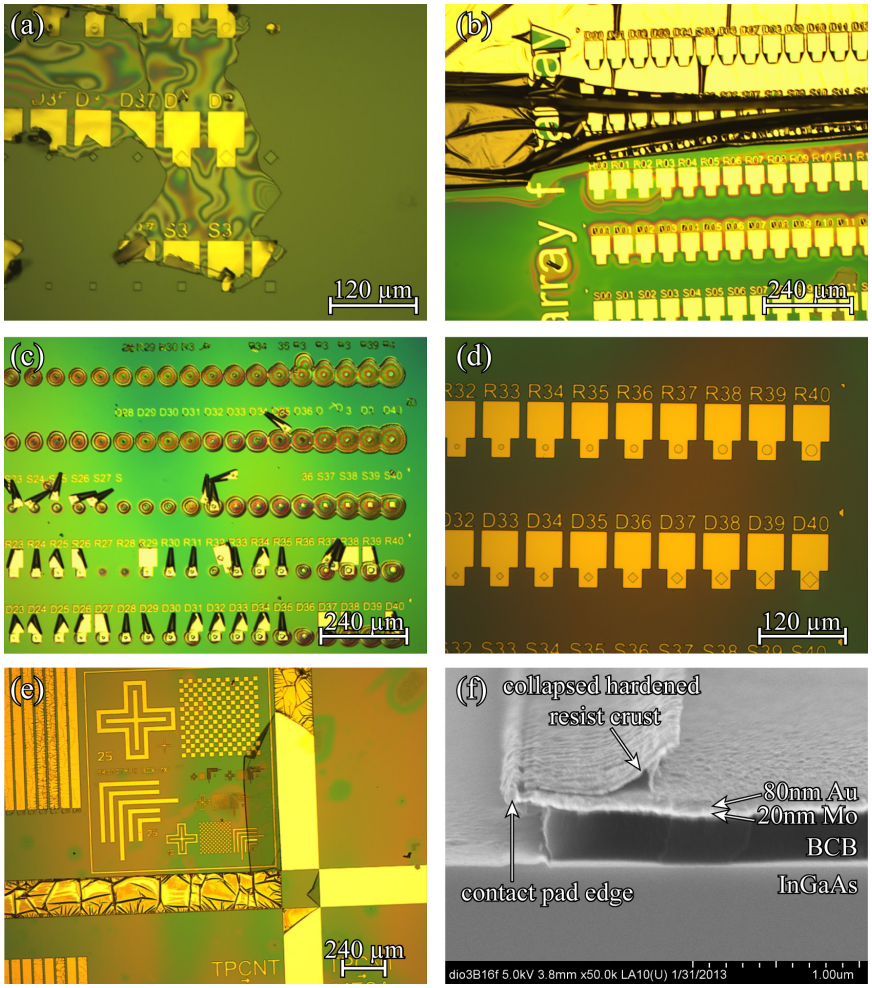


Figure C.12: Top contact patterning failed using liftoff for 12 hours in either (a) MS2001, or (b) acetone at 50°C, or (c) OPD5262. (d) The metal patterning is successful after ion milling, but the resist must still be removed. (e) Resist removal in acetone at 50°C failed, because (f) the XSEM image at edge of topcontact shows a hardened resist crust is still present.

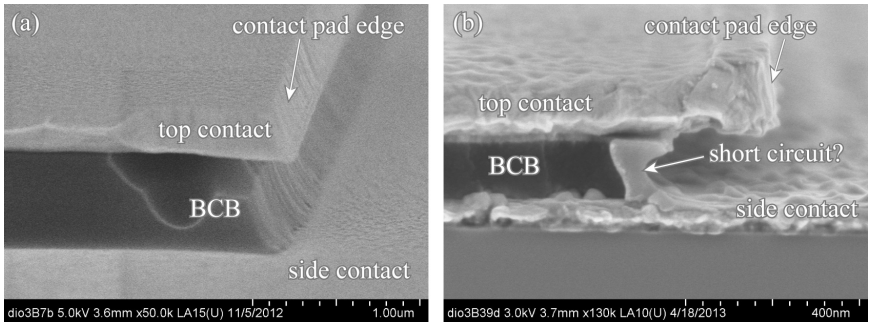


Figure C.13: (a) The BCB adjacent to the top contact pads is recessed to reveal the side contact underneath. (b) The BCB is overetched to reveal a metal particle bridging the top and side contacts.

in figure C.2(i), and by SEM in figure C.13(a). The recess is done in the *ML200RF* RIE tool with the following recipe: 180 cm^3/min O_2, 50 cm^3/min SF_6, 300 mtorr, 150 W for 120 s.

Even when no side contact is present, this second BCB recess is necessary to prevent a parasitic current path. This leakage current is observed by performing DC electrical measurements between two contact pads with no diode underneath, before the BCB recess. After BCB recess, the leakage current disappears. We presume the leakage path is due to incomplete ion milling in the previous processing step. Therefore, all diodes discussed in this thesis have received this second BCB recess, even when no side contact is present.

In many wafers we observe a persistent short circuit between the top contact and side contact after opening the latter. We determined that this short circuit only occurs when the recessed BCB thickness is thinner than ≈250 nm and a side contact is present. The exact cause of this problem could not be established, but we presume metal is bridging both contacts inside the BCB or at the edges of the contact pad, as shown in figure C.13(b). This problem can be avoided by either not using a side contact, or using a BCB layer thicker than 300 nm.

C.15 Conclusions

In conclusion, we have developed a new process flow, designed for the fabrication of Esaki diodes. It features wet etched diode mesas with diameters from 200 nm to 15 µm, defined by e-beam lithography. The n+$In_{0.53}Ga_{0.47}As$ at the top of

each diode is connected to a large $50\times50\mu m^2$ contact pad, to allow comfortable contacting with a probe needle and allow automatic measurements. The flow also features a self-aligned metal deposition on the exposed p+$In_{0.53}Ga_{0.47}As$ next to the diodes mesas, which can be contacted directly. Alternatively, the bottom part of the diode can be probed using a contact on the back of the p-type InP substrate.

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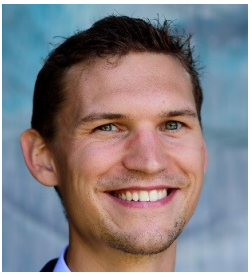

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